Duty-cycle Controlled Variable Gain Amplifier

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Outline

• Motivation
• Concept of the DC-VGA
• Design of the DC-VGA
• Simulation results
• Conclusions and future work
Motivation

• Read-out circuit for portable medical applications.
• Reduce steps (analog blocks) for signal conditioning.
• Adaptable gain and BW.
• Provide a suitable voltage range for the next block, e.g. ADC.
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Amplification based on inestability

Concept of the DC-VGA

\[ K = \exp \left( \frac{t_G}{\tau} \right), \quad 0 < t \leq t_G \]

When negative

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Proposed implementation of the DC-VGA
Timing diagram (1)

Concept of the DC-VGA

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Timing diagram (2)

Concept of the DC-VGA

\[ T_s \]

\[ T_{\text{clk}} \]

\[ T_R \]

\[ \phi_R \]

\[ \phi_S \]

Sampling \((T_s)\)

\[ V_{\text{in}} \]
Timing diagram (3)

Concept of the DC-VGA

Amplification ($T_A$)
Timing diagram (3)

Concept of the DC-VGA

Amplification ($T_A$)
Timing diagram (4)

Concept of the DC-VGA

Timing diagram:
- \( T_{\text{clk}} \)
- \( T_R \)
- \( T_S \)
- \( T_A \)
- \( V_{\text{out}} \)

Hold (\( T_H \))
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DC-VGA schematic including AZ loop

Design of the DC-VGA

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Two input-port OTA schematic

Consider:

- $G_m$
- Linearity
- Offset / $A_v$
- Power
- $f_k$ / Area
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OTA $G_m$ and linearity

Simulation results

$I_{out}$ [μA] vs $V_{in}$ [V]

$Gm1 = 370$ μS

$Gm2 = 37$ μS

$±120$ mV @ 5% error
MC simulations for the OTA

- Linearity error and $G_{m1}$ variation represents a max Gain error of 5%.
- The offset variation was the expected during design stage.
Output voltage signal obtained from the DC-VGA
Comparison of the response without AZ loop
Variable gain by duty-cycle

Simulation results

Gain [V/V] vs. Duty-cycle (%)

$T_A$
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Conclusions and future work

- A VGA controlled by duty-cycle was presented. Simulated post-layout results proved that it is suitable for amplification of biomedical signals.
- Some improvements in power consumption and area can be done depending on the application.
- Waiting for prototype to be tested inside AGC for biomedical signals.
Thank you for your attention