Ultra-low-power 2.4 GHz Colpitts oscillator based on double feedback technique

Rodrigo Eduardo Rottava*, Carlyle Câmara S. Jr.*, Fernando Rangel de Sousa* and Robson Nunes de Lima†
*RFIC Research Group - Electrical Engineering Department
Federal University of Santa Catarina
Florianópolis, SC, Brazil
Email: {rodrigorottava, carlyle.camara, rangel}@ieee.org
† Federal University of Bahia - UFBA
Email: robsonufba@gmail.com

***Abstract*— This paper presents an oscillator design technique for low-power applications. The circuit is based on the common-gate Colpitts oscillator with additional positive feedback provided by an inductive gate degeneration. This technique decreases the required transconductance to start-up oscillations, which makes possible to reduce the power consumption. Two prototypes were designed in a standard 0.18 μm CMOS technology. The first one presents an oscillating frequency of 2.52 GHz with a phase noise of -122.5 dBc/Hz at a 3 MHz offset frequency and consumes 120.8 μW. The other oscillator has a power consumption of 1 mW and oscillates at 2.38 GHz with a phase noise of -132.7 dBc/Hz at a 3 MHz offset.**

I. Introduction

The generation of reference signals is one of the most important steps in any communication channel. That relevance impose stringent requirements on the design of radio-frequency oscillators, which means they should both present a high spectral purity and consume as least power as possible. However, the natural compromise between performance and power consumption also dominates the design of oscillators. Although the phase noise could appear as the main concern related to oscillators, there are applications in which the limited power budget may deserve more attention from the circuit designer. This condition is even more demanding in the context of energy harvesting applications [1].

Several techniques have been proposed to cope with the challenging task of designing oscillators with increased performance and lower power consumption [2] - [6]. In [2], they employ a noise filter to reduce the phase noise of voltage-controlled oscillators (VCOs) to its fundamental minimum according to the resonator quality factor and power consumption. The oscillators designed in [3] make use of a tail capacitance for filtering the current source noise altogether with a DC level shift that enables a large oscillation amplitude, while the core transistors operate in the saturation region. [4] presents a transformer-feedback VCO based on the concept of dual signal swings, allowing the output signals to swing above the supply voltage and below the ground potential, which increases the carrier power and decreases the phase noise. A similar idea is shown in [5], in which they replace the tail current of a traditional differential Colpitts VCO by inductors to augment the maximum attainable amplitude. In [6], the author uses a cross-coupled MOSFET pair with forward-body bias to boost the negative conductance of a millimeter-wave differential Colpitts oscillattor.

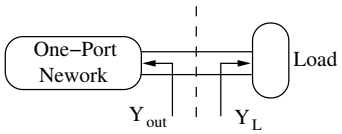


Fig. 1. Negative conductance high-level model of the Colpitts oscillator.

The current state-of-the-art CMOS oscillators have already demonstrated outstanding overall performance, but they still usually exhibit a DC power in the order of a few miliwatts [2], [3], [5], with some exceptions only [4]. In this paper we present a technique to design ultra-low-power oscillators implemented by means of an inductive gate degeneration applied to a classical Colpitts common-gate oscillator. The double feedback technique (DFT) reduces the required transconductance to start-up and maintain oscillations, thus saving power. Two prototypes were designed in a standard 0.18 μm CMOS technology as proof os concept. The simulation results indicate that the first one has an oscillation frequency of 2.521 GHz and a phase noise of -122.5 dBc/Hz at a 3-MHz offset frequency, with a power consumption of 120.8 μW from a 0.575-V supply voltage, which results in a figure-of-merit (FoM) of 190.2 dBc/Hz. The second oscillator consumes 1 mW from a 1-V supply voltage and presents a phase noise of -132.7 dBc/Hz at a 3 MHz offset, oscillating at 2.38 GHz, which corresponds to a FoM of 190.5 dBc/Hz. Those numbers represent the average values obtained through Monte Carlo simulations.

The rest of this paper is organized as follows: in section II, we introduce the basic ideas behind the low-power oscillators designed; section III makes a careful analysis of the additional positive feedback source and characterizes how it helps to minimize the required power to sustain oscillations; then we comment on some design insights regarding the implementation of the oscillators in IV; section V presents the main simulation results to validate the proposed approach, including

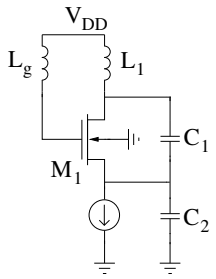


Fig. 2. Gate-inductive degenerated oscillator.

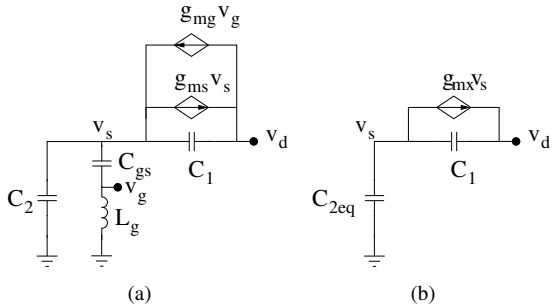


Fig. 3. Small-signal models of the proposed oscillator: (a): simplified model of circuit in Figure 2; (b): equivalent model to ease the analysis.

Monte Carlo analysis; finally section VI summarizes the most relevant contributions of this paper.

II. Gate-Inductive Degenerated Oscillator

The topology proposed derives directly from the classical Colpitts common-gate oscillator, which is shown in Figure 1 in a high-level model and can be seen as a combination of a potentially unstable one-port and a load network. Y_{out} is the one-port network output admittance and Y_L is the load admittance. In order to satisfy the Barkhausen criteria and start oscillations, the magnitude of the negative conductance represented by the one-port circuit must be greater than the conductance of the terminating load admittance, and the one-port susceptance must be the opposite of the load susceptance at the oscillation frequency. An amplifier is usually used as the one-port network and its nonlinearity provides the mechanism by which the oscillation amplitude stabilizes.

In the circuit of Figure 2, we show a Colpitts oscillator including inductive gate degeneration provided by L_g. This inductor acts as a second source of positive feedback, meaning that this topology is able to start oscillations with less power than the traditional Colpitts oscillator, as it is proved by the analysis conducted in the next section.

III. Circuit Analysis

Figure 3(a) shows the small-signal representation of the oscillator in Figure 2. In order to simplify the analysis, we have assumed that the drain transconductance (g_{md}), as well as the gate-to-drain capacitance (C_{gd}) of the transistor can be neglected, which is suitable for a saturated transistor. Under these conditions, we can relate the source and the gate transconductances as $g_{mg} = g_{ms}/n$, where n is the slope factor of the transistor, which is modeled according to the EKV MOSFET model [7]. It is also possible to write the gate voltage v_g in terms of the source voltage v_s, L_g and the gate-to-source capacitance C_{gs}. We define β as the source-to-gate voltage gain, which is given by:

$$\beta \doteq \frac{v_g}{v_s} = \frac{\omega^2 L_g C_{gs}}{\omega^2 L_g C_{gs} - 1} \tag{1}$$

The signal at the gate is phase-shifted in 180° with respect to the signal at the source when the oscillation frequency is below the resonant frequency of the series association between L_g and C_{gs}. In that case, the gate transconductance g_{mg} contributes to increase the magnitude of the output conductance seen at the drain.

Using the dependence between the gate and source voltages, the total transconductance controlled by the source voltage is given by:

$$g_{mx} = g_{ms} - \beta g_{mg} = g_{ms}\left(1 - \frac{\beta}{n}\right) \tag{2}$$

Finally, the total equivalent capacitance formed by C_2, C_{gs} and L_g is defined as C_{2eq}, and given by:

$$C_{2eq} = C_2 + \frac{C_{gs}}{1 - \omega^2 L_g C_{gs}} \tag{3}$$

By using these transformations, we can redraw the small-signal model of Figure 3(a) as the one in Figure 3(b). Using the expression for the output admittance Y_{out} obtained in [8], we have:

$$\begin{aligned} Y_{out} \quad &= -\frac{g_{mx}\frac{C_1}{C_{2eq}}}{\left(1+\frac{C_1}{C_{2eq}}\right)^2+\left(\frac{g_{mx}}{\omega C_{2eq}}\right)^2} \\ &\quad + j\frac{\omega C_1\left(1+\frac{C_1}{C_{2eq}}\right)}{\left(1+\frac{C_1}{C_{2eq}}\right)^2+\left(\frac{g_{mx}}{\omega C_{2eq}}\right)^2} \end{aligned} \tag{4}$$

Figure 4 depicts the output admittance given by (4) as a function of L_g for several values of C_2, considering the parameters of our second design. In this simulation we used g_{ms} = 13.9 mS, n = 1.15, C_{gs} = 2 pF, which is imposed by an additional capacitor, and C_1 = 2 pF. As we can see in Figure 4(a), the output conductance has one minimal for each C_2, but the absolute minimum value occurs for C_2 = 0.

For the component values above, and for C_2 = 0, the output conductance for a classical Colpitts oscillator, which has L_g = 0, would be -3.3 mS. It should be noted that although C_2 = 0, C_{2eq} is not, and thus the circuit still behaves as a Colpitts oscillator.

By choosing L_g = 2.63 nH and for the same passive devices and bias condition, the value of the output conductance falls to -15 mS. In other words, by keeping the same power consumption, the oscillator with inductive gate degeneration can drive a higher load than the classical Colpitts oscillator, or alternatively by fixing the load the present topology consumes less power than the classical one. The load admittance Y_L is considered as $-j/(\omega L_1) + G_P$, where G_P is the loss conductance due to the passive devices.

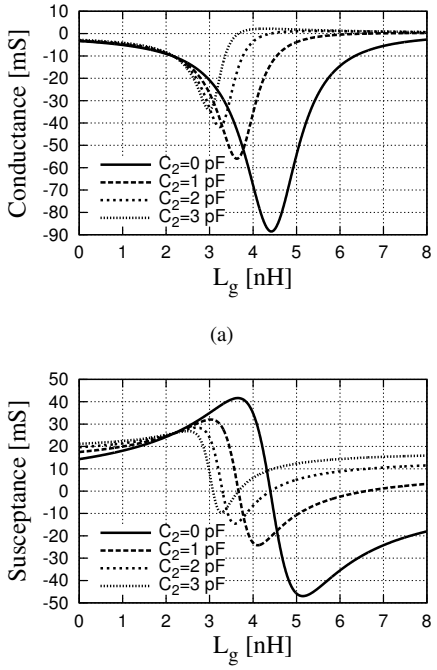


Fig. 4. Effect of gate inductor on one-port's: (a): output conductance; (b): output susceptance.

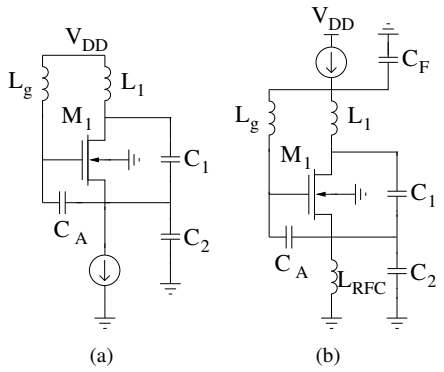


Fig. 5. Schematic diagram of designed oscillators: (a): design 1; (b): design 2.

It is important to observe in Figure 4 that the minimum output conductance for a given C_2 is close to an abrupt variation of the output susceptance, which means that a slight variation of the parameters can make the circuit oscillate at another frequency, or even not oscillate. In order to avoid this condition, we have chosen to work at the left side of the curve and slightly distant from the resonance point. Therefore, the output susceptance is capacitive and resonates with L_1 at the oscillation frequency, which is calculated as:

$$f_o = \frac{1}{2\pi\sqrt{L_1 C_{eq}}} \tag{5}$$

where C_{eq} is the total output capacitance given by $\Im\{Y_{out}\}/\omega$.

IV. Circuit Design

In order to validate the concept proposed, two prototypes were designed in the IBM 0.18 μm CMOS process. The first one, shown in Figure 5(a), was designed to keep the DC power as low as possible and consists basically of the oscillator in Figure 2 modified by an extra capacitor C_A. The second circuit is depicted in Figure 5(b) and was designed for a minimum phase noise, with a higher power consumption than the first one, but still lower than the typical values found in literature. Both oscillators are current-biased, because that way we can control the power consumption directly by changing the bias current.

The inductor was designed such its maximum Q-factor occurs near the oscillation frequency. For that, its outer diameter, number of turns, line width and line spacing were adequately chosen. In addition, the transistor gate-to-source capacitance was artificially raised to reduce the gate inductor value, because better quality factors were reached for smaller inductances. As the core transistors were laid out as multifinger devices, the impact of the internal gate inductance will be minimized.

V. Simulation Results

In this section we present the post-layout simulation results. The layout of both oscillators is shown in Figure 6. The circuits are still in the fabrication process, and we could not include the measurement results in this version of this paper.

It is difficult to compare the performance of different oscillators in a normalized sense. The most widely adopted definition of a figure-of-merit for oscillators is:

$$FoM = 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log\left(\frac{P_{DC}}{1\ mW}\right) - L(\Delta f) \tag{6}$$

where f_o is the oscillation frequency, P_{DC} is the DC power consumption and $L(\Delta f)$ is the phase noise at a Δf offset frequency.

It should be noted that the passive components from the adopted process are satisfactorily modeled, since previous characterizations were performed in our research group, and the measured values agreed quite well with the expected ones. That contributes to indicate that the measured performance will not deviate too much from the simulations presented here.

Table I shows the Monte Carlo simulation results including the maximum, minimum, mean and standard deviation for the two designed oscillators. The simulation was performed for 200 samples. As can be seen the worst FoMs are 188.6 and 189.1 dBc/Hz for the first and second oscillators designed, respectively. Since the tow oscillators operate in the current-limited regime, the performance could still be improved a little further, but at the cost of power consumption. In Table II we compare the average values of our results with some state-of-the-art CMOS oscillators. Our overall performance is comparable to them, however the design 1 has the lowest power consumption (120.8 μW).

TABLE I

RESULTS OF THE MONTE CARLO SIMULATION (200 RUN).

	Design 1				Design 2			
Parameter	FoM (dBc/Hz)	f_o (MHz)	P_{DC} (μW)	L(1 MHz) (dBc/Hz)	FoM (dBc/Hz)	f_o (MHz)	P_{DC} (mW)	L(1 MHz) (dBc/Hz)
Mean	190.2	2521	120.8	-122.5	190.5	2380	1	-132.7
Sigma	0.56	17.75	3.33	0.71	0.53	28	0	0.48
Max	191.4	2569	128.9	-120.9	192	2440	1	-131.4
Min	188.6	2468	114.4	-123.9	189.1	2310	1	-133.8

TABLE II

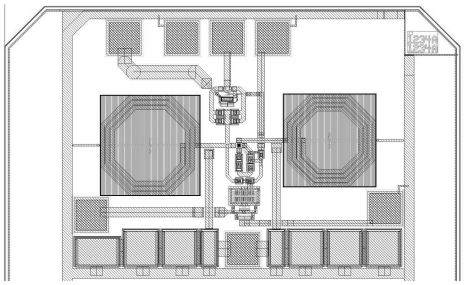
COMPARISON WITH STATE-OF-THE-ART CMOS OSCILLATORS

Parameters	[2]	[3] (RC bias)	[3] (TX bias)	[4]	[5]	Design 1	Design 2
CMOS Technology (nm)	350	130	130	180	130	180	180
Supply Voltage (V)	2.7	1.0	1.0	0.50	0.475	0.575	1.0
Frequency (GHz)	2.1	4.9	4.9	3.8	4.9	2.52	2.38
DC Power (mW)	9.3	1.4	1.3	0.57	2.7	0.1208	1
Phase Noise (dBc/Hz)	-153^1	-132.8^1	-132.8^1	-119^2	-136.2^1	-122.5^1	-132.7^1
FoM (dBc/Hz)	195.4	195.5	196.0	193	196.2	190.2	190.5

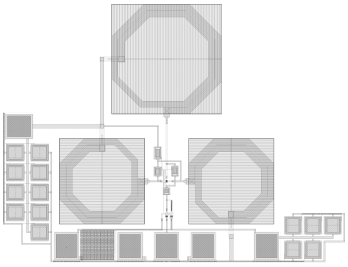
[1] @ 3 MHz, [2] @ 1 MHz

VI. CONCLUSION

This paper introduced the double feedback technique to minimize the power consumption of CMOS oscillators. The topology presented is based on the classical Colpitts common-gate oscillator, but it uses an inductive gate degeneration as a second source of positive feedback. Two prototypes were designed in a standard 0.18 μm CMOS process and Monte Carlo simulations showed the usefulness of the proposed technique to minimize the DC power required to start-up and sustain oscillations. The first oscillator presents an oscillation frequency of 2.521 GHz and a phase-noise of -122.5 dBc/Hz at a 3 MHz offset frequency and consumes 120.8 μW, which indicates a FoM of 190.2 dBc/Hz. The second oscillator consumes 1 mW and oscillates at 2.38 GHz with a phase-noise of -132.7 dBc/Hz at a 3 MHz offset frequency, exhibiting a FoM of 190.5 dBc/Hz.



(a)



(b)

Fig. 6. Layout of the two prototypes: (a): design 1; (b): design 2.

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