

# A 2.4GHz Cascode CMOS Low Noise Amplifier

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## ABSTRACT

A cascode CMOS low noise amplifier (LNA) is presented along with the used design methodology and measurement results. The LNA works at 2.4 GHz with 14.5 dB voltage gain and 2.8 dB simulated noise figure (NF). Powered from a 1.8 V supply, the core measured current consumption is 2.76 mA. An output buffer was designed to match a  $50\ \Omega$  load and its current consumption is 5.5 mA. The technology used was a standard  $0.18\ \mu\text{m}$  CMOS.

## 1. INTRODUCTION

Applications such as sensor networks and portable devices usually communicate with frequencies at the Industrial, Scientific and Medical (ISM) band. These systems are getting smaller and are being powered by small batteries or energy scavenging techniques, such as harvesting from radio frequency signals, temperature gradient or motion and vibration [9]. Therefore, it is important to develop small and efficient communication devices. One important building block of such systems is the low noise amplifier (LNA), which must have low power consumption and a reduced footprint.

The LNA is one of the first building blocks on the majority of receivers. Its main purpose is to provide gain while preserving the input signal-to-noise ratio at output, which is an important characteristic because the received signals are, usually, weak and can be in presence of a great amount of interference [5].

It is usual to design LNAs using a single transistor configuration [5] and there are three possibilities for such LNAs, since one of the transistor nodes is AC grounded. These possibilities are presented in Figure 1. The common-source amplifier (Figure 1a) is usually the driver of an LNA, but it has poor reverse isolation. The common-drain (Figure 1b) is often used as a buffer, since its voltage gain is close to unity. The common-gate (Figure 1c) configuration can also be used as an amplifier by itself, but it is usually employed as an isolation stage in high frequency LNAs.

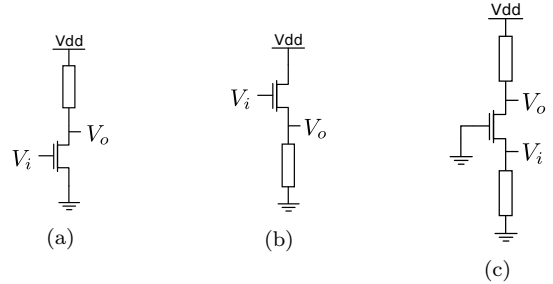


Figure 1: Possibilities of single transistor amplifier: (a) common-source; (b) common-drain; (c) common-gate

Due to device limitations, other structures, more complex than the single transistor ones, can be chosen [3, 5]. One of these structures is the cascode topology and it is a combination of the common-source and the common-gate amplifiers. The cascode topology is one of the most common configurations for LNA design. This topology is usually chosen because it can be used up to higher frequencies. The cascode transistor reduces the Miller effect on capacitor  $C_{gd1}$  of the common-source stage by reducing its voltage gain. It happens because the impedance seen from the drain of the first transistor is approximately  $1/g_{ms2}$ , impedance of cascode transistor's source, which is usually lower than the amplifier load. In this way, it is possible to maintain the LNA's gain at higher frequencies as well as to assure its stability. One drawback of the cascode topology is its reduced linearity. It happens due to the stacking of two transistors, which reduces the available output voltage swing. Also, the cascode LNA cannot be as low noise as a single transistor LNA, because the common-gate stage adds more noise to the amplifier [5].

This paper presents the design and measurement results of an LNA using the cascode topology, developed in a standard CMOS  $0.18\ \mu\text{m}$  technology, operating with a frequency of 2.4 GHz. In the next section, the design methodology, some simulation results and layout are presented. The third section presents the results of measurement and comparison with simulation results. The fourth section shows a conclusion of the work.

## 2. DESIGN

The chosen topology for the developed LNA is the cascode common-source presented in Figure 2. The amplifier core consists of transistors  $M_1$  and  $M_2$  and the tank circuit ( $C_T$

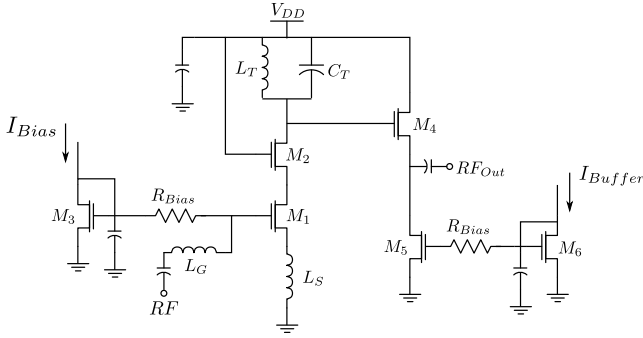


Figure 2: LNA's schematic with buffer

Table 1: Component values

Component	Value
$M_1$ and $M_3$	$W = 46.5 \mu\text{m}, L = 0.18 \mu\text{m}$
$M_2$	$W = 114 \mu\text{m}, L = 0.18 \mu\text{m}$
$M_4, M_5$ and $M_6$	$W = 28 \mu\text{m}, L = 0.18 \mu\text{m}$
$L_S$	1.44 nH
$L_G$	20.27 nH
$L_T$	3.58 nH
$C_T$	1.04 pF
Other capacitors	7.83 pF
$R_{BIAS}$	6.25 k $\Omega$

and  $L_T$ ). The transistor  $M_3$  is responsible for the amplifier biasing. The purpose of inductors  $L_G$  and  $L_S$  is matching the input with  $50 \Omega$ . The degeneration inductor  $L_S$  also trades gain for linearity. The transistors  $M_4$ - $M_6$  form a buffer, included to allow the on-wafer characterization of the LNA using a  $50 \Omega$  based setup. Resistors  $R_{Bias}$  are used to block the influence of RF signals on biasing. Other capacitors are used to block DC or act as part of low pass filter on bias circuits. All the component values are presented in Table 1.

The design methodology chosen is divided in four steps described as following [5]:

**Step 1: find the transistor's current density that will provide the lowest minimum noise figure (NF).**

A change in biasing has effect on the noise at the output of the amplifier and to achieve the lowest possible noise, the right current density must be found. Different technologies have different optimum current densities and this step must be performed for each one.

To understand the variation of noise with the bias current consider (1), (2) and (3), which give the noise power at the output of the common-source amplifier for noise due to gate resistance, drain channel noise and gate induced noise, respectively [5].

$$v_{no,rg}^2 \approx 4kTr_g g_{m1}^2 R_L^2 \quad (1)$$

$$v_{no,id}^2 \approx 4kT\gamma g_{m1}^2 R_L^2 \quad (2)$$

$$v_{no,ig}^2 \approx \frac{4}{5}kT\delta\omega^2 C_{gs1}^2 g_{m1}^2 R_L^2 \quad (3)$$

where  $r_g$  is the gate resistance,  $T$  is the temperature,  $k$  is the Boltzmann constant,  $R_L$  is the amplifier load,  $\gamma$  is the

excess-noise factor, its value is  $2/3$  for long channel transistors in strong inversion,  $\omega$  is the angular frequency of the signal and  $\delta$  is a correction factor, its value is  $4/3$  in strong inversion.

Comparing the variation of the noise power to the signal power, where the signal power is given by

$$P_{out} = \frac{v_{out}^2}{R_L} = g_m^2 v_{in}^2 R_L,$$

the influence of current  $I_D$  on the NF can be evaluated. For instance, the noise due to gate resistance (1) is proportional to the current, using the simple square law model ( $g_m \propto \sqrt{I_D}$ ). Since the output power is proportional to  $g_m^2$ , the NF is not sensitive to this noise source when  $I_D$  changes. On the other hand, drain channel noise and gate induced noise, (2) and (3), are proportional to  $\sqrt{I_D}$ . Thus, increasing the current reduces the NF. This result is true for low values of  $I_D$ , but as  $I_D$  is increased an optimal point of the NF is revealed. The increase in NF for higher  $I_D$  is observed due to effects that were not considered, such as the increase of  $\gamma$  with bias current [5]. These effects are better considered in the more complex models used by simulators [2][8].

Through simulation, the current density ( $I_D/W$ ) that produces the lowest NF for the used technology was  $60 \mu\text{A}/\mu\text{m}$ .

**Step 2: choose the dimensions of the transistor that makes the real part of the optimum source impedance for lowest NF equal to  $50 \Omega$ .**

The NF changes with source impedance and there is an optimum impedance that gives the minimum NF, as is explained by the classical noise theory, and given by [3]:

$$F = F_{min} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2$$

where  $Y_{opt} = G_{opt} + jB_{opt}$  is the optimum source admittance, calculated as

$$G_{opt} = -B_c$$

$$B_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2}$$

where  $R_n$  is an equivalent noise source resistance,  $Y_u$  and  $Y_c$  are equivalent admittances for uncorrelated and correlated noise sources, respectively, and  $Y_s$  is the source admittance. If  $Y_s = Y_{opt}$ ,  $F$  becomes  $F_{min}$  and, consequently,  $NF = NF_{min}$ . Since the source impedance is  $50 \Omega$  in this design,  $Z_{opt} = 1/Y_{opt}$  must be set to  $50 \Omega$ . This can be achieved by choosing an adequate value for the width of  $M_1$  (the length is always equal to  $L_{min}$  to achieve the highest  $f_t$ ), since  $Y_c$ ,  $Y_u$  and  $R_n$  depend on the transistor dimensions.

In this design step, current density of  $M_1$  ( $I_{D1}$ ) must be kept at its optimal to preserve the lowest noise. This is achieved by using a current  $I_{Bias} = W_1 I_{D1}$  and mirroring it to  $M_1$ , this is done with  $M_3$ . To avoid mismatch, its dimensions of  $M_3$  was set equal to those of  $M_1$ . The dimensions of the transistors are summarized in Table 1.

**Step 3: place and size  $L_S$ , the source degeneration inductor, so that the real part of the input impedance is  $50 \Omega$ .**

The approximated input impedance expression, with both inductors placed, is

$$Z_{in}(s) = \frac{1}{sC_{gs1}} + s(L_S + L_G) + \frac{g_{m1}}{C_{gs1}}L_S \quad (4)$$

The use of inductive degeneration, performed by  $L_S$ , will modify the real part of the input impedance, as can be seen in (4). Thus, there is a value of  $L_S$  that corresponds to  $\Re\{Z_{in}\} = 50 \Omega$  and it was found to be equal to 1.44 nH.

**Step 4: place and size the inductor  $L_G$  in series with the gate so that the imaginary part of the input impedance is zero.**

To cancel the imaginary part of  $Z_{in}$ , we need to set the value of  $L_G$  as

$$L_G = \frac{1}{\omega^2 C_{gs1}} - L_S$$

There may be a combination of  $C_{gs1}$  and  $L_S$  that results in an impractical value of  $L_G$ . When this happens, one possible solution is to reduce the value of  $C_{gs1}$ , which can be achieved by folding the transistor  $M_1$ . In our case, the value found for  $L_g$  was 20.27 nH.

After adding the cascode transistor and the tank circuit resonating in 2.4 GHz, the simulated voltage gain of the LNA, without the buffer, is 29 dB and its output impedance is  $360 + j29 \Omega$ .

In order to connect a  $50 \Omega$  measurement instrument, we had to include an output buffer, so that the gain was not degraded. The buffer consists of a source follower, which has a current mirror as a load. The current fed to the buffer's current mirror is 2.75 mA. The simulated buffer attenuation is 10 dB.

The Figure 3 presents the simulation results regarding the noise figure. The NF gets close to the minimum NF near the operation frequency (2.4 GHz). In this frequency the NF is equal to 2.8 dB and the minimum NF is 2.0 dB. These values were obtained through post-layout simulation. A difference between the NF and minimum NF appears due to parasitics that were not considered, such as the inductor series resistance and coupling between inductors that are close to each other.

The implemented layout is presented in Figure 4. The total area of the layout with the pads is  $506 \mu\text{m} \times 821 \mu\text{m}$  ( $0.42 \text{ mm}^2$ ) and the area without the pads is  $265 \mu\text{m} \times 580 \mu\text{m}$  ( $0.15 \text{ mm}^2$ ). The inductors used are single metal layer inductors, made with the last layer of metal. The capacitors are dual MIM (Metal-Insulator-Metal), which are composed of two parallel MIM capacitors, increasing the capacitance density. The transistors used are RF transistors, each one with its own guard ring. The layout was designed for on-wafer characterization so that the RF terminals ( $RF_{in}$  and  $RF_{out}$  in Figure 4) are composed of three pads for probing with a ground-signal-ground RF probe. In this kind of probe, the signal is inserted in the middle pad while the other two pads are connected to ground.

The results of post-layout simulation, with extracted para-

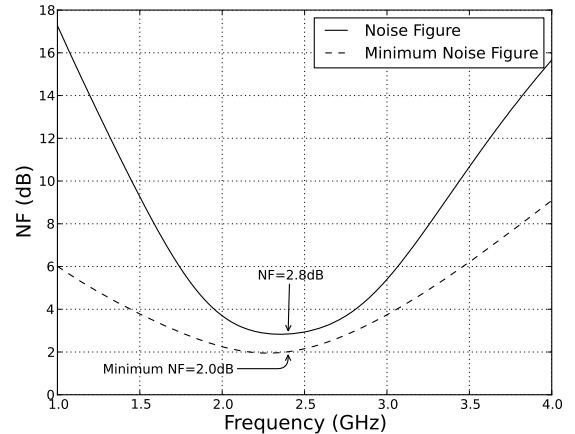


Figure 3: NF simulation results

Table 2: Summary of post-layout simulation results at 2.4 GHz

Parameter	Value
$S_{21}$	16.8 dB
$S_{12}$	-45 dB
$S_{11}$	-23.3 dB
$S_{22}$	-16.2 dB
NF	2.8 dB
IIP3	-6.6 dBm
Power (total)	19.8 mW
Power (core)	5 mW

itics, are summarized in Table 2. Some of these results are compared to the measured ones in the next section.

### 3. RESULTS

The measurements were done on chip using a microprobing station, RF and DC probes, a semiconductor parameter analyzer (HP4145), used to set the bias, and a vector network analyzer (Rohde & Schwarz ZVB8), used to verify the S-parameters and linearity.

The Figure 5 presents the S-parameter curves, from post-layout simulation and measurements, with the input signal frequency varying from 1 to 4 GHz. Discrepancies between the simulated and measured S-parameters are due to imperfections of the used models of components and connections, which are exacerbated in high frequency. For instance, there was a frequency shift between the simulated and measured values of  $S_{11}$ , which was probably occasioned by discrepancies in  $L_G$ ,  $L_S$  or  $C_{gs1}$ . It is also observed some discrepancies in the parameters  $S_{21}$ ,  $S_{12}$  and  $S_{22}$ , but they are still at acceptable levels. By analyzing the data on Figure 5a, it can be found that the 3-dB bandwidth of the LNA is approximately 330MHz.

The Figure 6 is a micrograph of the fabricated LNA taken during the measurements, where all the probes necessary to apply the bias and to do the measurements are placed.

The linearity can be verified through Figure 7. The 1-dB

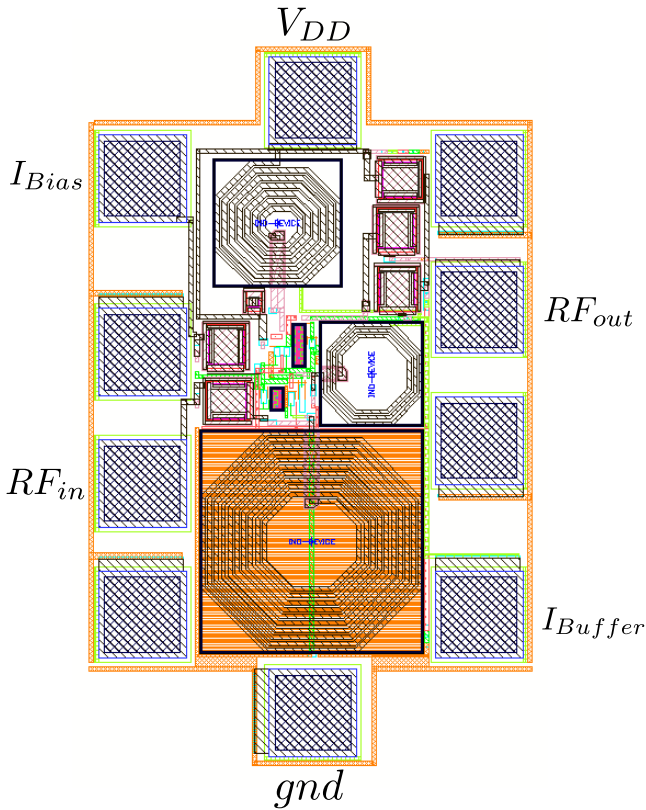


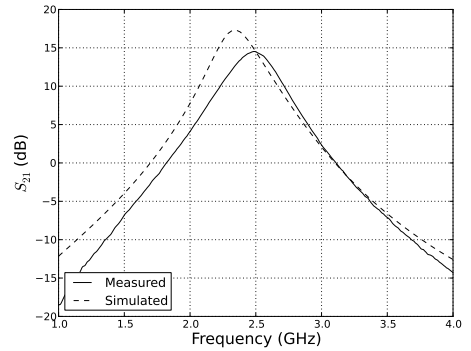
Figure 4: Layout of the LNA

compression point is located at  $-17.5$  dBm of input power. The IP3 related to the input calculated from the IP1 value was  $-7.8$  dBm.

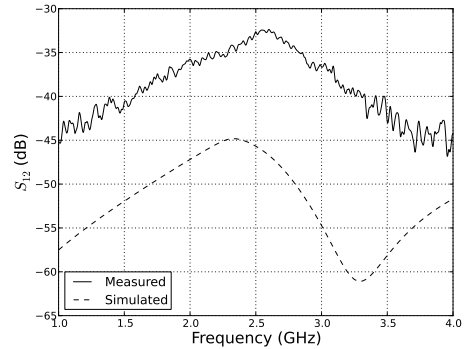
The Table 3 shows a comparison with other LNAs in recent works. These LNAs have operating frequencies near 2.4 GHz and were designed with comparable technologies, but they have some different characteristics. The amplifier shown in [1] is inductorless with differential input and output. The results presented in [4] are simulation only and the IIP3 on the table is calculated based on the given 1-dB compression point. The topology of the LNA in [4] is a cascode common source with no source degeneration inductor. The LNA shown in [6] is a cascode common-source. The LNA in [7] is reconfigurable, the highest gain point is considered. The topology in [10] is a cascode with a common source second stage. The LNA of this work has advantages in comparison to the others presented here, such as a small footprint while keeping low NF and high voltage gain. This work makes a balance between these three figures of merit. The IIP3 also has a high value if compared to others.

#### 4. CONCLUSION

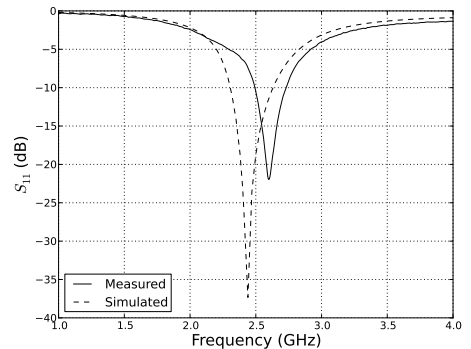
A 2.4 GHz cascode common-source LNA was designed in a standard  $0.18 \mu\text{m}$  CMOS technology. The LNA presented has 14.5 dB gain, 2.8 dB NF and  $-7.8$  dBm IIP3 in a  $0.15 \text{ mm}^2$  area. The amplifier core consumes 5 mW with 1.8 V supply voltage. This LNA has a relatively small area and power consumption. It also works in the ISM band, making it suitable to a large range of applications.



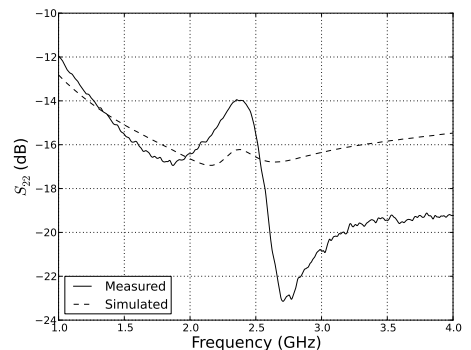
(a)



(b)



(c)



(d)

Figure 5: Simulated and measured curves of: (a)  $S_{21}$  (b)  $S_{12}$  (c)  $S_{11}$  (d)  $S_{22}$

Table 3: Comparison between 2.4GHz CMOS LNAs

Parameter	[1]	[4]	[6]	[7]	[10]	This Work
Gain (dB)	20	15	4.5	14.6	23	14.5
NF (dB)	4	3.6	2.77	3.8	3.8	2.8
IIP3 (dBm)	-12	-14.3	11.8	-12	-9.1	-7.8
Core power consumption (mW)	1.32	0.8	18	0.12	13	5
Area (mm <sup>2</sup> )	0.007	-	0.55	-	4.1	0.15
Supply voltage (V)	1.2	0.8	1.8	0.6	1.0	1.8
CMOS technology	0.13 $\mu$ m	0.13 $\mu$ m	0.18 $\mu$ m	0.13 $\mu$ m	0.18 $\mu$ m	0.18 $\mu$ m

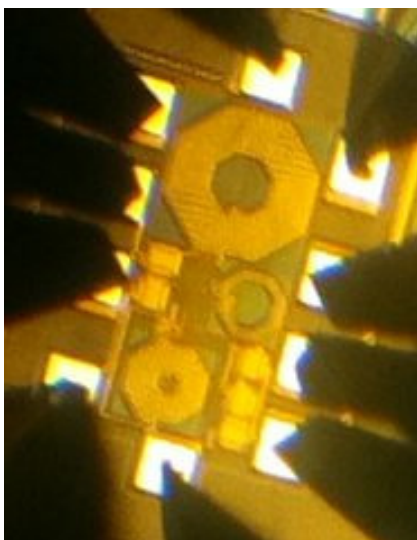
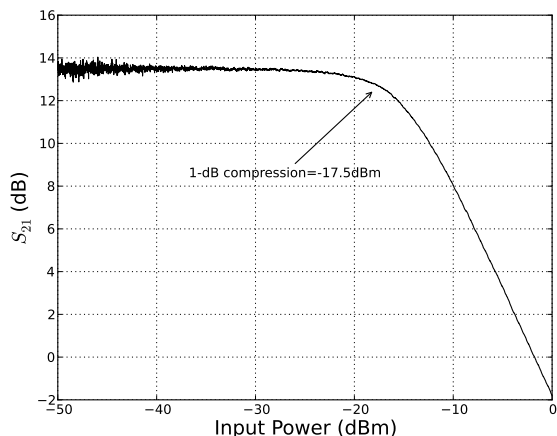


Figure 6: A micrograph of the LNA during tests

Figure 7: Linearity analysis:  $S_{21}$  versus input power

There were some discrepancies between the simulated and measured S-parameters, specially  $S_{11}$ , which were probably due to the inefficiency in high frequency of the component models used in simulation. The other S-parameters still remained in acceptable levels.

## 5. ACKNOWLEDGMENTS

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