Integrated CMOS Class-E Power Amplifier for Self-Sustaining Wireless Power Transfer system

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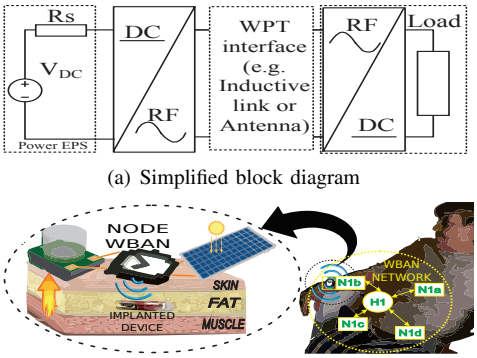
***Abstract*—In this paper is proposed a methodology for designing a CMOS class-E PA used to drive an inductive link. In order to satisfy the operating conditions imposed by the PA specifications and the available technology, a differential class-E PA with split slab inductor and high level of integration was both designed and simulated. The proposed methodology uses the analytical solution of the ideal class-E PA equations as the first point of an iterative procedure for solving the optimization of the PA. Further, the proposed design set solve the trade-off between ON-resistance and gate capacitance of the switches, resulting in the optimal choice of the power transistors width for a class-E PA with finite DC-feed inductance. In the post-layout simulation, the PAE of the PA was 45.7% when 20.7 dBm.**

Keywords*—Class-E, power amplifier, power efficiency, wireless power transfer.



(a) Simplified block diagram

(b) for powering implanted device

Fig. 1. Self-sustaining WPT system

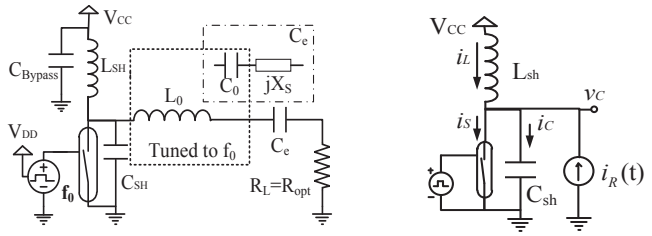
I. Introduction

Currently, there is an increasing interest in providing energy autonomy to electric devices in order to implement concepts such as the Internet of Things (IoT), and Wireless Body Area Networks (WBAN) [1]–[3]. Energy-harvesting technologies allow this autonomy, collecting energy from primary energy-sources (e.g. solar, thermal, kinetic, or electromagnetic). When energy in the environment are insufficient, secondary energy-sources are used to power the self-sustaining device. For instance, a satellite collects solar energy and then radiates this energy to other satellites where it can be used [4]. On a smaller scale, the non-electromagnetic energy sources and wireless power transfer (WPT) have been used to synthesize artificial energy sources [5]. This kind of scheme, illustrated in the Fig. 1(a), is referred as self-sustaining WPT systems. The integrated power amplifier (PA) proposed in this paper is part of a self-sustaining WPT system for powering an implanted device, this concept is shown in the Fig. 1(b).

Integrating a PA in a CMOS system-on-chip is challenging, mainly due to the low breakdown voltage of CMOS devices and low quality factor (Q) of the integrated passive components (i.e. inductors with low Q). Several approaches have been used in order to increase the power added efficiency (PAE). For instance in [6], it was explored the analytical solution of the trade-off between the ON-resistance and gate capacitance for finding the transistor size that maximizes the PAE of a integrated class-D PA. As another example, in [7], it was implemented a PA with high PAE using an Class-E power oscillator with injection-locking and only the transistor integrated (i.e. passive components off-chip). This system incurs in a significant penalty of area, cost, and hardware complexity. As an intermediate solution between area and efficiency (η), the use of the bond-wire connections as inductances was reported in [8]. But, the inductance values are limited and not well controlled. On the other hand, in [9], it was proposed a fully-integrated class-E PA with high PAE using an on-chip slab inductor combined with an adaptive class-E PA.

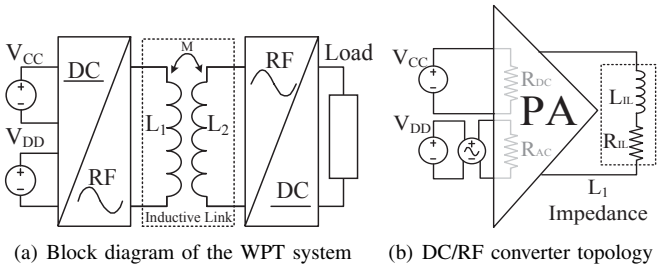
The Class-E PA with a finite dc-feed inductance instead of an RF-choke has been explored in several works [10]–[13]. This topology is shown in the Fig. 2(a). For the same supply voltage, output power and load, using finite dc-feed inductance has significant benefits [12]: more efficient output matching network, implementation in low-voltage technologies and higher frequency of operation. The published papers design the PA based on analytical equations or based on iterative procedures [13]. Further, when the switch on-resistance and the inductor resistance are taken into account, the class-E PA solution (i.e. the optimum operation of the non-ideal PA for maximum η) results in nonlinear analytic equations that must be solved numerically [11] or in iterative design procedures even more lengthy and complex [14]. Furthermore, this solution occurs outside the nominal operation of the class-E PA (i.e. ZVS and DZVS) [14]. As an alternative option, the methodology proposed in this paper uses an analytical design set for calculating the start point of an optimization process, hence its complexity decrease.

In this work a methodology for designing a CMOS class-E PA that drives an inductive link is proposed. This methodology uses an expanded version of the Class-E design set proposed in [10]. This set solves the trade-off between ON-resistance and gate capacitance of the switches, resulting in a suboptimal

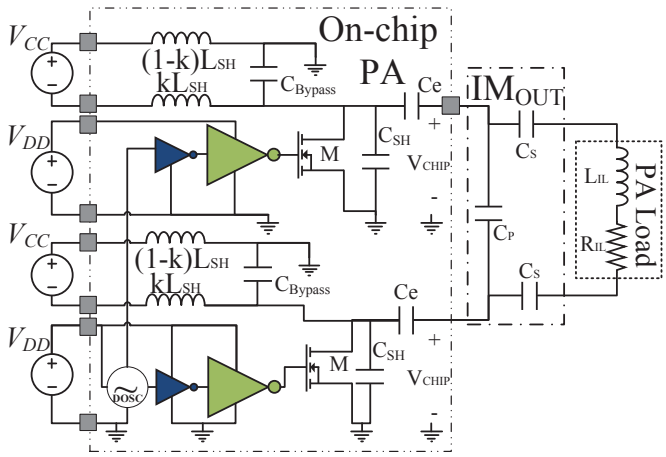


(a) Ideal model (b) Ideal model with high Q

Fig. 2. Class-E PA with a finite dc-feed inductance



(a) Block diagram of the WPT system (b) DC/RF converter topology



(c) Topology of the diferencial Class E PA with split slab inductor

Fig. 3. System description a top-down approach

choice of the power transistors width, near to its optimum value. In order to satisfy the operating conditions imposed by the PA specifications (e.g. load and source impedance are not equal to 50 Ω) and the available technology (i.e. 180nm), a differential class-E PA with split slab inductor was designed and simulated. In the post-layout simulation, the PAE of the PA was 45.7% when 20.7 dBm was delivered to its load.

II. PA Design

The power amplifier (PA) proposed in this paper is part of a self-sustaining WPT system for powered an implanted device. This system transfers energy from a wireless body area network (WBAN) node to an implanted device, as illustrated in Fig. 1(b). To achieve energy autonomy, the WBAN node harvest energy from the body environment (i.e. solar and thermal energy) for powering two DC/DC converters which in turn powered the DC/RF converter. The WPT interface is implemented with an inductive link, where the harvested energy is transferred through magnetic coupling between two inductors: the primary inductor is connected to the source and the secondary is embedded into an implanted device. The inductive link needs an RF signal which frequency must be chosen to optimize the link efficiency [15]. The system can be summarized as shown in Fig. 3(a). The implementation of the DC to RF converter is based on an oscillator that drives a switched PA as shown in the Fig. 3(b).

A. PA Specifications

PA Load: The PA proposed was designed for driving an inductive link whose primary inductor is described in [6]. The secondary side is a fully-integrated wireless power receiver explained in [16]. The power delivered to the primary inductor was specified to be at least 20 dBm at a frequency of 990 MHz (f_0). The inductive link is expected to operate under the weak coupling regime, for this reason the input impedance of the link is approximately the impedance of the primary inductor. This impedance can be represented as an inductor ($L_{IL} = 9.3nH$) in series with a resistor ($R_{IL} = 1.8\Omega$), as presented in Fig. 3(c).

PA Energy Source: The power supply will be a multi-input energy-harvesting system with solar and thermal energy inputs, intermediate storage, shared inductor, and regulated outputs ($V_{DD} = 1.8V, V_{CC} \leq 1.8V$). The topology will be similar to the proposed in [17].

General: The PA must has high efficiency, narrow band operation and high level of integration. Additionally, in order to avoid extensive electromagnetic simulations, only the available components of the design kit were used. The principal limitations of these technology are: $V_{nom} = 1.8$ V, $V_{I/O} = 5$ V, $L_{min} = 180$ nm, $IL_{DC_{max}} = 150$ mA, $IL_{RMS_{max}} = 228$ mA, $L_{SH} < 2$ nH, $C_{SH} > 10$ pF.

B. Proposed PA Topology

The diagram of the proposed differential class-E PA is shown in Fig. 3(c). The capacitors C_S and C_P form an impedance transformation network (IM_{OUT}). The capacitor C_S must be off-chip because the voltage at load-terminals exceeds the maximum value of the chip technology. The equivalent capacitance C_e combines the impedance jX_s and C_0 at the operation frequency (Fig. 2(a)). On the other hand, the choice of the C_e integration (Fig. 3(c)) has at least two advantages [6]: 1) low harmonic level at the chip output, which is translated into lower power losses. 2) higher output voltage, which means a reduction in the output current for the same power level and hence lower losses in the wire-bond parasitic resistance. In order to provide flexibility to the design, the C_P will be an external device that allows to adjust the resonance of the load and the unmodeled parasitic capacitances. This capacitive value is limited by the output PAD and wire-bond capacitances. The DC energy sources of the amplifiers do not share the same reference, hence the inductor L_{SH} may be split ($k \leq 1$). The advantages of this approach are: 1) simplify the layout when slab inductors are implemented, 2) decrease both gain reduction and source degeneration. The transistors (M in Fig. 3(c)) act as switches, its widths (W) are in the order of mm, therefore its gate capacitance is high, given that the use of drivers are necessary. In the chip a differential oscillator ($DOSC$) and a driver (i.e. Two cascaded inverters) are integrated.

C. Ideal PA model

The PA was analyzed by its half-circuit shown in Fig.2(a). The transistor is represented as an ideal switch. The ideal class-E can be modeled as the circuit shown in Fig. 2(b) when the control signals have zero time transitions at a frequency f (near to f_0) and the series resonant circuit L_0, C_e and R_L has a high loaded quality factor. Therefore, the output current is given by (1). As a result of development presented in [10], for ideal class-E nominal operation (i.e. with ZVS and DZVS), the PA currents and PA voltages, are given by the equations (2) to (7).

$$i_R(t) = I_P sin\left(\omega t + \varphi\right) = \sqrt{\frac{2P_{OUT}}{R_L}} sin\left(2\pi f t + \varphi\right); \quad (1)$$

$$v_{C_{SH\,on}}(t) = i_{C_{SH\,on}}(t) = i_{S_{off}}(t) = 0; \quad (2)$$

$$i_{L_{SH\,on}}(t) = \frac{V_{CC}}{L_{SH}} t - I_P sin\left(\varphi\right); \quad (3)$$

$$i_{S_{on}}(t) = \frac{V_{CC}}{L_{SH}} t + I_P\left(sin\left(\omega t + \varphi\right) - sin\left(\varphi\right)\right); \quad (4)$$

$$i_{L_{SH\,off}}(t) = \frac{V_{CC}}{L_{SH}} t - \int_{\frac{2\pi D}{\omega}}^{t} \frac{v_{C_{SH}}(\tau)}{L_{SH}} d\tau - I_P sin\left(\varphi\right); \quad (5)$$

$$v_{C_{SH\,off}}(t) = V_{\mathrm{CC}} + \begin{array}{c} C_1 \cos(q\omega t) + C_2 \sin(q\omega t) \\ -\frac{q^2}{1-q^2} p V_{\mathrm{CC}} \cos(\omega t + \varphi); \end{array} \quad (6)$$

$$i_{C_{SH\,off}}(t) = \begin{array}{c} \frac{V_{CC}}{L_{SH}} t - \frac{1}{L_{SH}} \int_{\frac{2\pi D}{\omega}}^{t} v_{C_{SH}}(\tau) d\tau \\ +I_P\left(sin\left(\omega t + \varphi\right) - sin\left(\varphi\right)\right) \end{array}; \quad (7)$$

where, X_{on} means that the expression X is valid when the switch is in the ON state ($0 < t < \frac{2\pi D}{\omega}$). On the other hand, X_{off} means that the expression X is valid when the switch is in the OFF state ($\frac{2\pi D}{\omega} < t < \frac{2\pi}{\omega}$). The constants C1 and C2 are analytic functions of p,q,φ and V_{DD}, and they were found in [10]. The variables p and q were introduced by [10], in order to simplify the math analysis and are defined as:

$$q = \frac{1}{\omega\sqrt{L_{SH} C_{SH}}} = \frac{\omega_{SH}}{\omega}; p = \frac{\omega L_{SH} I_P}{V_{CC}} = \frac{Z_{L_{SH}}}{R_\omega}; \quad (8)$$

where, ω_{SH} is the natural frequency of the LC_{SH} network , Z_{LSH} is the impedance of L_{SH}, and R_ω is:

$$R_\omega = \frac{V_{CC}}{I_P} = \sqrt{\frac{P_{in} R_{DC}}{2P_{out}/R_L}} = \frac{\sqrt{R_L R_{DC}}}{\sqrt{2}}; \quad (9)$$

where, R_L is the PA load , P_{in} is the power delivered by V_{CC}, P_{out} is the power dissipated by R_L, and R_{DC} is the equivalent resistance that the amplifier imposes to V_{CC}, introduced by [18]. It can be calculated as:

$$R_{DC} = \frac{V_{DC}}{I_{DC}} = V_{CC} \Big/ \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{\omega}} i_s(t) dt = \frac{R_\omega}{g}; \quad (10)$$

from (10) and (9), we find $R_{DC} = R_L/2g^2$, where

$$g(q, D) = \left\{ \begin{array}{c} \left(\frac{1-\cos(2\pi D)}{2\pi}\right)\cos\left(\varphi\right) \\ +\left(\frac{\sin(2\,\pi\,D)}{2\pi} - D\right)\sin\left(\varphi\right) + \frac{D^2\pi}{p} \end{array} \right\}. \quad (11)$$

TABLE I. LOSSES PARAMETERS

Parameter h
$h(D,q) = \begin{array}{c} h_0(D,q) + \frac{2}{p}\left\{h_1(D,q)\cos\left(\varphi\right) + h_2(D,q) sin\left(\varphi\right)\right\} \\ +h_3(D,q)\cos\left(2\varphi\right) + h_4(D,q) sin\left(2\varphi\right) \end{array}$ Where, $h_0(D,q) = \frac{8}{3}\frac{D^3\pi^3}{p^2} + 2\pi\,D - \sin\left(2\,\pi\,D\right)$ $h_1(D,q) = \sin\left(2\,\pi\,D\right) - 2\,\pi D\cos\left(2\,\pi\,D\right)$ $h_2(D,q) = \cos\left(2\,\pi\,D\right) + 2\,\pi D\sin\left(2\,\pi\,D\right) - \left(1 + 2\,D^2\pi^2\right)$ $h_3(D,q) = \sin\left(2\,\pi\,D\right) - \frac{1}{4}\sin\left(4\,\pi\,D\right) - \pi\,D$ $h_4(D,q) = -2(\sin\left(\pi D\right))^4$
Parameters P_{SS}
$P_{ss_1}(q,D) = \frac{g(q,D)}{p(q,D)}\left((2p(q,D)g(q,D))^2 + (\pi D)^2\right)$ $P_{ss_2}(q,D) = \frac{2}{\pi} g(q,D)\sqrt{h(q,D)}$

It is important to emphasize that the expressions from (1) to (11) can be calculated in terms of V_{CC}, ω, R_L, and P_{OUT} only if p,q,φ and D are known, but in [10] was demonstrated that both φ and p could be solved as an analytic function of both q and D. Additionally, the peak value of the v_C must be less than the breakdown voltage of M. In [13] is proposed a simple analytic relationship between the DC input voltage and the peak value of the v_C. This expression was based in the numerical solution of the analytical equations of the ideal class-E proposed by [10], [12]. This relationship is:

$$V_{c_{max}} \approx V_{CC}\left(\frac{1.83}{1-D}\right). \quad (12)$$

D. Modeling losses and sizing the transistors

Assuming the same waveforms of the ideal PA and modeling M as an ideal switch and a series resistance (R_{on}), and L_{SH} as an ideal inductor and a series resistor (R_{SH}), the power dissipated (P_{Loss}) can be approximated by:

$$P_{Loss} = P_{L_{SH}} + P_{R_{on}} + P_{driver}; \quad (13)$$

$$P_{L_{SH}} = {i_{L_{rms}}}^2 R_{SH}; \quad (14)$$

$$P_{R_{on}} = {i_{S_{rms}}}^2 R_{on} = {i_{S_{rms}}}^2 \frac{b}{W}; \quad (15)$$

$$P_{driver} = {V_{DD}}^2 f \alpha C_G = {V_{DD}}^2 f \alpha a W; \quad (16)$$

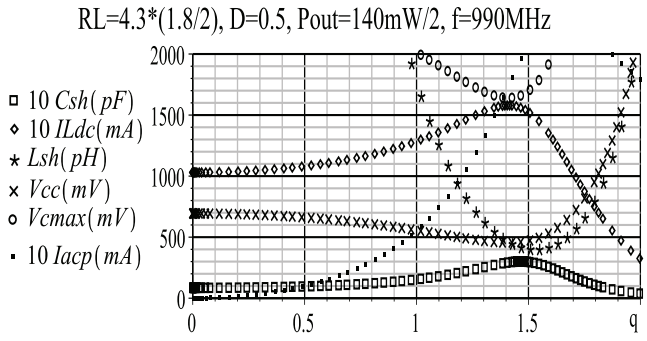
where, P_{SH} is the power dissipated by R_{SH}, $P_{R_{on}}$ is the power dissipated by R_{on}, a and b are technology parameters introduced in [19], P_{driver} is the power used to charge and discharge the NMOS gate capacitance C_G, and the factor α represents the capacitance excess due to the driver implementation. Hence, solving the trade-off between the ON-resistance and the gate capacitance, the W that minimize (13) is:

$$W = \frac{\sqrt{a/b}}{V_{DD}} \sqrt{\int_0^{\frac{1}{f}} i_s(t)^2 dt} = \frac{g(D,q)}{1\Big/\sqrt{h(D,q)}} \frac{2V_{CC}\sqrt{\frac{b}{a\omega}}}{R_L V_{DD}}; \quad (17)$$

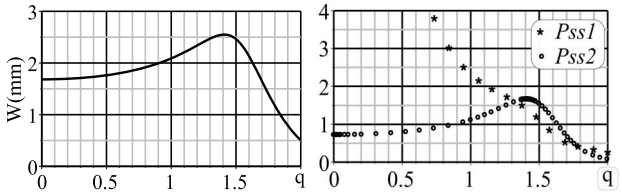
therefore, the minimum losses are given by:

$$P_{LOSS} = \frac{{V_{CC}}^2}{R_L}\left(P_{SS1}\frac{1}{Q_{L_{SH}}} + P_{SS2}\frac{\sqrt{\alpha a b}\sqrt{\omega}}{V_{CC}/V_{DD}}\right); \quad (18)$$

where $Q_{L_{SH}}$ is the quality factor of the L_{SH}, and all the loss parameters (i.e. h, P_{SS_1} and P_{SS_2}) are listed in the Table I. For $D = 50$ %, the P_{SS} functions are plotted in the Fig.4(c),



(a) Design space of the Class E PA with split slab inductor



(b) Optim. $W@P_L = 140$mW/2 (c) P_{SS} functions for D=50%

Fig. 4. Parametric sweep of q

it is clear that for high q values the driver losses are more significant than the inductor losses. Contrary, for low q values the inductor losses are significant. Further, both losses are quasi equals for the q near to 1.412, this q value maximize the output power [10].

E. Proposed design set

The relations between the input parameters (i.e. q, D, Q_L,and ω), the circuit element values (i.e L_{SH}, C_{SH}, C_e, L_0 and R_L), and the circuit specification (e.g. $I_{L_{DC}}$,$I_{L_{RMS}}$,R_{DC},P_{OUT},V_{CC}) should be known for calculating the PA design space. These relations are referred as the design set. in order to limit the calculated design space by technology constraints (e.g. RMS current in the inductor), we expanded the set proposed in [10]. This proposed set is summarized in the Table II. Further, their relations are illustrated in Fig.5. It is important to emphasize that the expressions summarized can be calculated only if p and φ are known, but both can be solved as analytic functions of both q and D. This set was implemented in the software Maple® in order to analyze all the involved trade-offs.

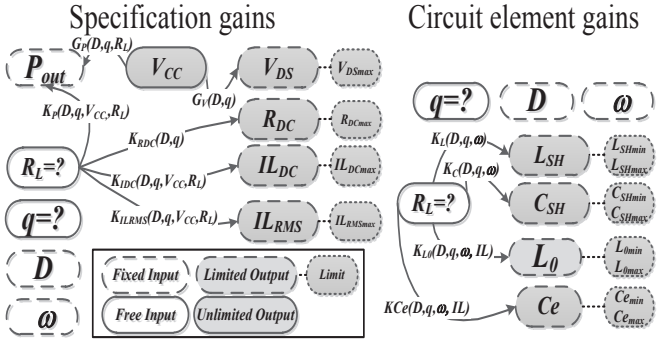


Fig. 5. Proposed design set

TABLE II. DESIGN SET GAINS

Circuit element gains
$K_P(q,D,V_{CC},R_L) = Pout/R_L = 2g(q,D)^2\left(\frac{V_{CC}}{R_L}\right)^2$
$K_{C^{-1}}(q,D,\omega) = (C_{SH})^{-1}/R_L = \frac{q^2 p(q,D)}{2g(q,D)}(\omega)$
$K_L(q,D,\omega) = L_{SH}/R_L = \frac{p(q,D)}{2\cdot g(q,D)}\left(\frac{1}{\omega}\right)$
$K_{X_S}(q,D) = \frac{X_s}{R_L} = \frac{v_{C_I}/i_{R_Q}}{v_{C_Q}/i_{R_Q}} = \frac{\left(\frac{-2}{I_P T}\int_0^T v_C(t)cos(\omega t+\varphi)dt\right)}{\left(\frac{-2}{I_P T}\int_0^T v_C(t)sin(\omega t+\varphi)dt\right)}$
$K_{L_0}^{-1}(\omega,Q_L) = L_0/R_L = \frac{Q_L}{\omega}$
$K_{C_0{}^{-1}}(\omega,Q_L) = (C_0)^{-1}/R_L = Q_L\omega$
$K_{C_e{}^{-1}}(\omega,Q_L,q,D) = (C_e)^{-1}/R_L = \omega\left(Q_L - K_{X_s}(q,D)\right)$
Specifications gains
$K_{R_{DC}} = R_L/R_{DC} = 1/2g(q,D)^2$
$K_P(q,D,V_{CC},R_L) = Pout/R_L = 2g(q,D)^2\left(\frac{V_{CC}}{R_L}\right)^2$
$K_{IL_{DC}}(q,D,V_{CC},R_L) = i_{L_{DC}}/R_L = 2g(q,D)^2\frac{V_{CC}}{R_L{}^2}$
$K_{IL_{RMS}}(q,D,V_{CC},R_L) = \frac{i_{L_{DC}}}{R_L} = \left(\begin{array}{c}4g(q,D)^4\\ +2\pi^2\left(\frac{g(q,D)\cdot D}{p(q,D)}\right)^2\end{array}\right)\frac{V_{CC}{}^2}{R_L{}^3}$
$G_P(q,D,V_{CC},R_L) = P_{out}/V_{CC} = 2g(q,D)^2\left(\frac{V_{CC}}{R_L}\right)$
$G_V(q,D) = v_{C_{max}}/V_{CC} \approx \left(\frac{1.83}{1-D}\right)$

F. Design Methodology Steps

1) Design class-E PA for nominal operation: Calculate the design space of the PA assuming an ideal class E PA, a drain efficiency value (i.e. $\eta = 70\%$), the proposed design set, the operating conditions and a given technology. In this phase, a value for q, D, and R_L that satisfies all the constraints must be identified. Parametric sweeps of the variables R_L and q were made for a fixed P_{out}. In the designed PA the value of D was chosen in order to simplify the design of the differential oscillator ($D = 50\%$). The possible R_L range was found (from 1.8 to 5). In Fig. 4(a) is shown the final sweep of the variable q with R_L fixed in its optimum value ($R_L = 3.87\ \Omega$), and a $P_{out} = 140/2$ mW (i.e $P_{out} = P_{in}\eta$). In the range $1 < q < 1.1$, all the goals of the analyzed PA are simultaneously achieved; in the superior limit of q, the DC current achieves its maximum possible value (i.e. 150 mA); in the inferior limit of q, the inductance and V_C values (2 nH and 2 V) are both limited by technology constraints. The q chosen was 1.05.

2) Estimate the Sizing of the transistors: Simulate or measure the transistors to obtain the parameters b and a of the technology. The parameters a and b were estimated by simulation using the MOSFET model ($b = 4.3\text{m}\ \Omega\cdot$ m, $a = 7.8$ nF/m). Assuming a driver overhead (i.e. $\alpha = 1.5$ overhead of 50%) estimate the optimal value for the transistor width using (17). In the Fig.4(b) is shown this optimum value for the PA as a q function, for $D = 50\%$, $R_L = 3.87\ \Omega$ and $P_{out} = 140$ mW.

3) Calculate impedance transformation network: Calculate the transformation network that transforms the load to the optimum load. Considering the Fig. 3, the capacitors C_S and C_P form an impedance transformation network (IM_{OUT}) that transforms R_{IL} and L_{IL} in R_{opt} and L_0 respectively. We calculate the capacitances (C_S, C_P and C_e) using the equations listed in the Table III. These equations were developed using a procedure similar to [6]. Further, the maximum voltage parameter (V_{max}) was set as 4 V because in the technology the allowed voltage for I/O is 5 V.

TABLE III. CAPACITANCE EXPRESSIONS

$$\frac{1}{C_S} = \omega^2 L_{LI} - \omega R_{LI}\sqrt{\left(\frac{{V_{\max}}^2}{2P_{out}R_{LI}} - 1\right)}$$

$$\frac{2}{C_P} = \frac{\omega\frac{Rs}{R_{opt}}\left(\left(\omega L_{LI} - \frac{1}{\omega C_S}\right)^2 + {R_{LI}}^2\right)}{\left(\omega L_{LI} - \frac{1}{\omega C_S}\right) - \sqrt{\left(\omega L_{LI} - \frac{1}{\omega C_S}\right)^2 \frac{R_{LI}}{R_{opt}} - {R_{LI}}^2 + \frac{{R_{LI}}^3}{R_{opt}}}}$$

$$\frac{1}{C_e} = \omega\left(\sqrt{\frac{R_{opt}}{4R_{LI}}\left(\left(\omega L_{LI} - \frac{1}{\omega C_S}\right)^2 - R_{opt}R_{LI} + {R_{LI}}^2\right)} - K_{X_S}R_{opt}\right)$$

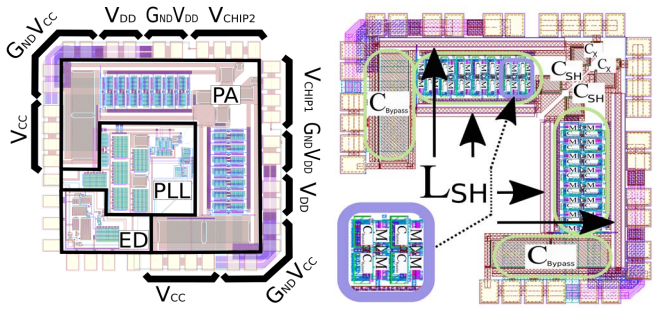
4) Optimization process: From an efficiency point of view, the nominal waveform (ZVS and DZVS) is optimum only if the parasitic components are negligible. For each circuit, the optimum occurs out of the nominal class-E operation. Therefore, the values computed in the previous steps are the initial values of the optimization process assisted by simulation. In the optimization process there are many interactions that are being adjusted. In the available design kit the models of the passive elements do not allow automation, therefore a suboptimal optimization was made, where parametric sweeps of some circuit values were used to find the local maximums of the goal function. These sweeps were performed in a predefined order with the available variables, e.g. in post-layout optimization only V_{CC} and the off-chip component values are available. The optimization process is summarized in the tables IV and V. In these tables the identifier *Opt* means that the set values presented was optimized, as well as *Vsin* or *Vpul* means that the PA was driven by a single-tone or a pulse-signal in the input of the driver for the pre-layout and post-layout simulations, or a single-tone or a pulse-signal in the gate of the transistors for the others simulations.

III. CMOS CLASS-E IMPLEMENTATION

As is shown in the Fig. 6(a), in addition to the PA, the chip includes a PLL for generating the differential input signal for the PA and an envelope detector (ED) to sense the backscattered response at the inductive link (their implementation is out of the scope of this paper). The implemented PA circuit is based on the diagram of Fig. 3(c). The PA pinout is shown in the Fig. 6(a). The PADs were organized in such way to facilitate the wirebonding process to the printed board. The detailed layout of the PA is shown in Fig. 6(b). Each transistor (M) and its driver were divided in sixteen cells. The channel length was 180 nm for all transistors, and their widths are summarized in the Table VI. The driver transistors were sized

TABLE IV. TABLE OF THE CHANGED CIRCUIT VALUES IN THE OPTIMIZATION

Name	q	V_{CC} (mV)	L_{SH} (nH)	Q	C_{SH} (pF)	Q	W (mm)	C_e (pF)	Q	C_P (pF)
Ideal	1,05	535	1,5	-	15,7	-	-	7,7	-	-
Integrated Lsh	1,05	535	1,44	17	15,7	-	-	7,7	-	-
Integrated Csh	1,05	535	1,50	-	15,9	98	-	7,7	-	-
Int. MOS W	1,05	535	1,50	-	15,7	-	2,63	7,7	-	-
Int. L,C and M	1,05	535	1,44	17	15,9	98	2,63	6,4	-	6,2
Int. L,C and M Opt.	1,10	600	1,40	17	14,6	105	2,27	6,3	185	6,2
Int. (L,C, M, Cx). Opt.	1,10	600	1,40	17	14,6	105	2,36	6,2	210	6,2
Int. (L,C, M, Cx). Vsin Opt.	1,10	600	1,40	17	14,6	105	3,87	6,2	210	6,2
PreLayout	1,10	600	1,22	15	14,8	57	4,56	6,2	210	6,2
PostLayout	1,10	600	1,22	15	14,8	57	4,56	6,2	210	6,2
PostLayout Opt.	1,10	660	1,22	15	14,8	57	4,56	6,2	210	5,8
PostLayout Vsin	1,10	660	1,22	15	14,8	57	4,56	6,2	210	5,8



(a) Blocks and pinout diagram (b) Detailed layout of the PA

Fig. 6. CHIP Layout

to drive the switches at the specified frequency considering that transitions must be slow while turning the switches on and fast while turning them off as is shown in the waveform plotted on the Fig. 7(a). Dual Metal-Insulator-Metal (MIM) bypass capacitors were included for the digital voltage source (V_{DD}) for filtering the supply voltage. They were divided and positioned near of each M cell in a routing star-like approach, in that way the AC current is well distributed.

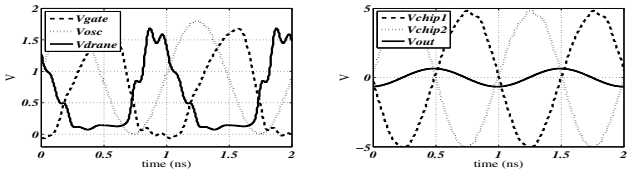
The capacitors C_e and C_{SH} were integrated using the MIM option which provides a higher quality factor than dual MIM option. The inductor L_{SH} was splitted using a $k = 0.612$ in order to simplify the layout. Each slab inductor was implemented in the last metal layer with the higher available width for the slab inductor model (i.e. $W = 25$ um for the used design kit) for high quality factor. The chip floorplanning was very important since the current through the V_{DD} supply nodes can be up to 220 mA rms, and a DC current of 150mA. Hence, a large number of PADs were used for source connections in order to reduce the parasitic impedance of the bondwire, and for increasing its current carrying capacity. For the bypass capacitors the Dual-MIM option was used for high density capacitance value in order to reduce the AC current on the voltage source.

TABLE V. TABLE OF THE MERIT FIGURES USED AS GOALS IN THE OPTIMIZATION

Name	P_L (mW)	η (%)	PAE (%)	R_{DC} W	V_{max} (mV)	$I_{L_{DC}}$ (mA)	R_L type
Ideal	148	99,9	99,9	3,89	2017	137	Ropt
Integrated Lsh	120	86,4	86,4	4,13	1833	129	Ropt
Integrated Csh	138	97,0	97,0	4,03	2063	133	Ropt
Int. MOS W	100	84,2	74,1	4,82	1662	111	Ropt
Int. L,C and M	80	72,1	55,3	5,13	1683	104	LI+IM
Int. L,C and M Opt.	106	73,0	61,5	4,98	1886	121	LI+IM
Int. (L,C, M, Cx). Opt.	100	66,1	55,3	4,75	1629	126	LI+IM
Int. (L,C, M, Cx). Vsin Opt.	114	62,8	62,3	3,99	1476	150	LI+IM
PreLayout	100,1	63	47,3	4,55	1854	132	LI+IM
PostLayout	83,77	59,8	42,2	5,14	1706	117	LI+IM
PostLayout Opt.	116,3	60,3	46,3	4,52	1659	146	LI+IM
PostLayout Vsin	117,5	59,4	45,7	4,41	1682	150	LI+IM

TABLE VI. THE WIDTHS OF TRANSISTORS OF THE PA

MOS Type	1th driver stage N	1th driver stage P	2th driver stage N	2th driver stage P	Switch (M) N
W (um)	2	4	2,48	2,48	2,85
Fingers	1	1	5	5	100
We (um)	32	64	198	198	4560



(a) MOS signals (b) Output voltages

Fig. 7. PA simulated waveforms

A. Simulated Results and State of Art

The designed PA was simulated using Cadence® Virtuoso® and Advanced Design System (ADS®). The circuit and the parasitic resistances and capacitances were extracted from the layout. The layout view of the PA is shown in Fig. 6. As shown in the Table IV, the calculated values of the circuit elements (Int. L,C and M) and the final values of the proposed PA (PostLayout Vsin) had good agreement, i.e. percentage change less than 20% in all circuit values except the V_{cc} and (W). The performance of the designed PA is compared with the PAs found in literature in Table VII. The efficiency achieved is the best between the references with integrated inductor. The simulated waveform of both the differential chip outputs and the load voltage is plotted in the Fig. 7(b). The voltage excursion of the PAD is between the designed specifications.

TABLE VII. COMPARISON TABLE OF THE PERFORMANCE

Ref	f (MHz)	P_L (dBm)	PAE %	Area (mm^2)	Tech. (nm)	R_L oms	$L_{DC_{feed}}$ type	PA class	Tested type
[7]	820	29	70,7	0,5	180	50	External	E	Exp.
[6]	990	25,1	58	1,5	180	1,8	w/o L	D	Sim.
This Work	990	20,7	45,7	1,5	180	1,8	On-chip Split L	E	Sim.
[8]	900	29,5	41	4	250	50	Bondwire	E	Exp.
[9]	800	28	40	1,5	180	50	On-chip Transformer	E	Exp.

IV. CONCLUSIONS

An analytic design methodology to find the optimum transistor width of a class-E PA was presented. An integrated differential class-E PA with split slab inductor was designed and simulated with good agreement between the initial values of the circuit elements (calculated), and the final values after the optimization process. Hence, the complexity of this process decreases thanks to the suboptimal first point found by the proposed analytical solution. In the post-layout simulations, the PAE of the PA was 45.7 % when 20.7 dBm was delivered to its load and a 2.3 dBm was supplied by the AC source. This good result was obtained thanks to the proposed design methodology. The PA designed in this work is highly integrated, only two capacitors are left outside the chip. The silicon area is kept small because the PA uses slab inductors and splitted inductor class E topology.

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