Integrated CMOS Class-E Power Amplifier for Self-Sustaining Wireless Power Transfer system

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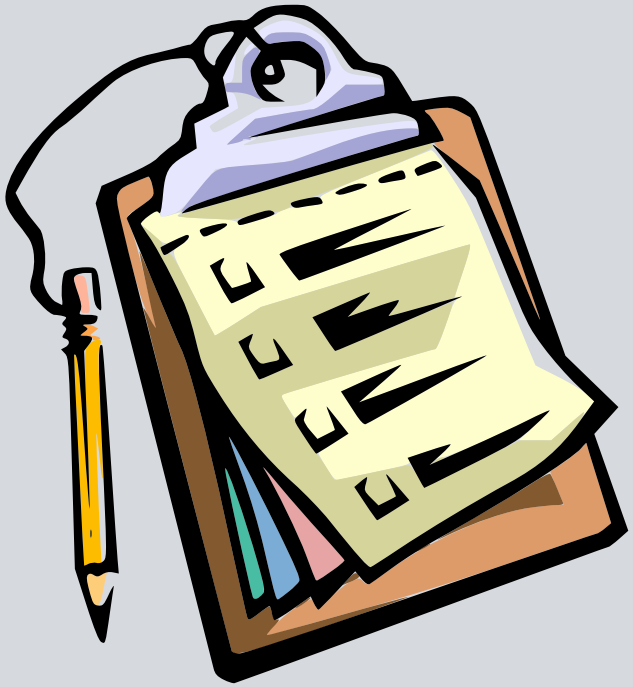
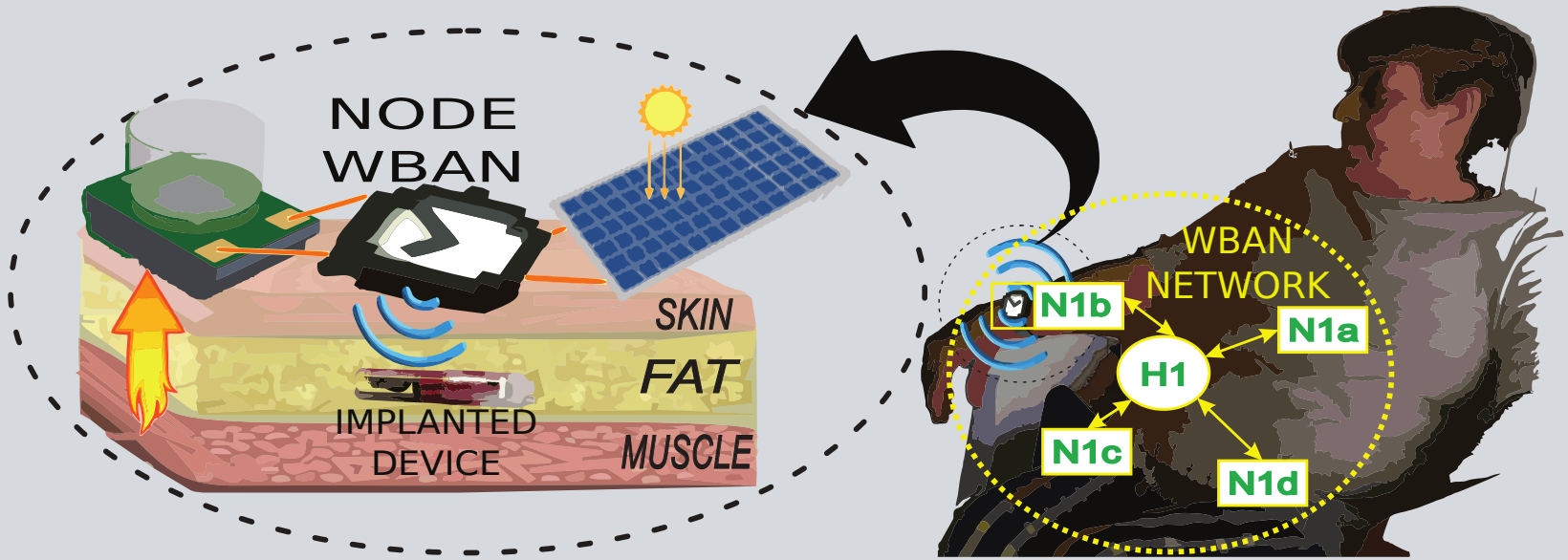
Agenda



- Introduction
- Proposed design methodology
- PA model and proposed design Set
- Study case Integrated class-E PA
- CMOS implementation
- Conclusions
- Acknowledgment
- References

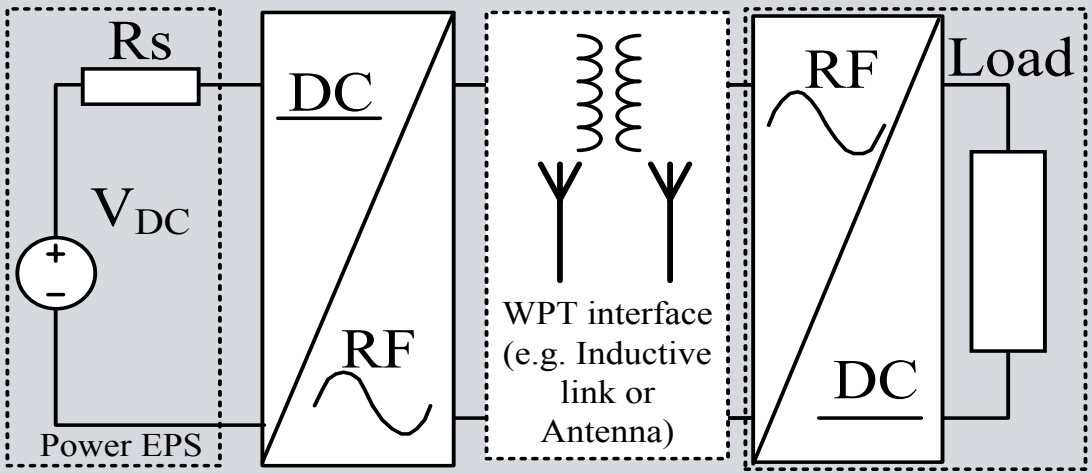
WPTn concept for implanted device autonomy

WPT node (WPTn) is an autonomous wearable WBAN node used as energy and communication solution for a passive implanted RFID tag that sense biomedical data.



Self-sustaining WPT system power chain

The maximum available power (P_{avs}) of the power supply in the implant is limited by BOTH the efficiency of the power chain and the P_{avs} of the Power EPS [1].



[1] A. Fajardo and F. Rangel de Sousa, "Ideal energy power source model and its implications on battery modeling", in *Proc. 22th IBERCHIP Workshop*, Florianopolis, Brasil. 2016, pp. 19–25.

Integrated Class E PA as WPT driver

- Integrating a switched PA is challenging, mainly due to the low breakdown voltage of CMOS devices and the low Q of the onchip passive components.
- An WPT driver was implemented as an oscillator that drives a Class D PA in [2].
- The Class-E PA with a finite dc-feed inductance (Class-E finLDC) could be full integrated [3].

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[2] F. Cabrera and F. Rangel de Sousa, "A 25-dbm 1-ghz power amplifier integrated in cmos 180nm for wireless power transferring", in *Integrated Circuits and Systems Design, 2016.Proceedings*, 2016.

[3] M. Acar, A. Annema, and B. Nauta, "Analytical design equations for class-e power amplifiers", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 12, pp. 2706–2717, 2007.

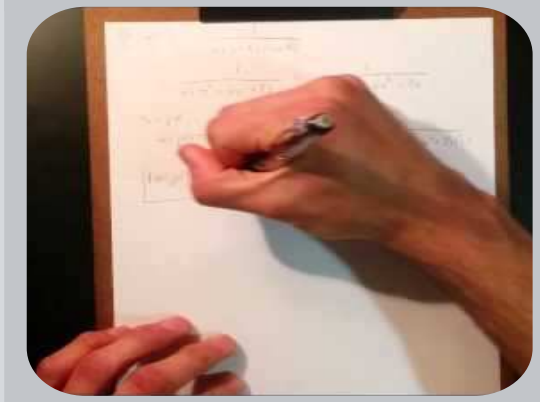
Design of Class-E finLDC

Most of the methodologies used for designing the Class-E PA with a finite dc-feed inductance involve hard simulation work [4] or numerical method solution of nonlinear equations [5].

[4] N. Sokal and A. Mediano, "Redefining the optimum rf class-e switch-voltage waveform, to correct a long-used incorrect waveform", in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2013, pp. 1–3.

[5] R. Sadeghpour and A. Nabavi, "Design procedure of quasi-class-e power amplifier for low-breakdown-voltage devices", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1416–1428, 2014.

Analytic Modeling of Class-E finLDC



The first analytical model of Class-E finLDC was proposed in [3][a] assuming ideal components and high loaded Q. In [5][b] the switch on-resistance and the inductor resistance are taken into account, the class-E PA solution results in nonlinear analytic equations that must be solved numerically.

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[a] M. Acar, A. Annema, and B. Nauta, "Analytical design equations for class-e power amplifiers", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 12, pp. 2706–2717, 2007.

[b] R. Sadeghpour and A. Nabavi, "Design procedure of quasi-class-e power amplifier for low-breakdown-voltage devices", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1416–1428, 2014.

Proposed PA Design Methodology

A low complexity methodology for designing a CMOS class-E PA that drives an inductive link under weak coupling is proposed.

Step 1- Calculate Design space

Consider the model proposed in [3] for calculating the design space. Then identify the values of the key model parameters that satisfies the design constraints.

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Simulate or measure the transistors for obtaining some technology parameters. Then estimate the transistor width using the ON-resistance and gate capacitance Trade-Off and choose the transistor length as the minimum allowed by the CMOS process.

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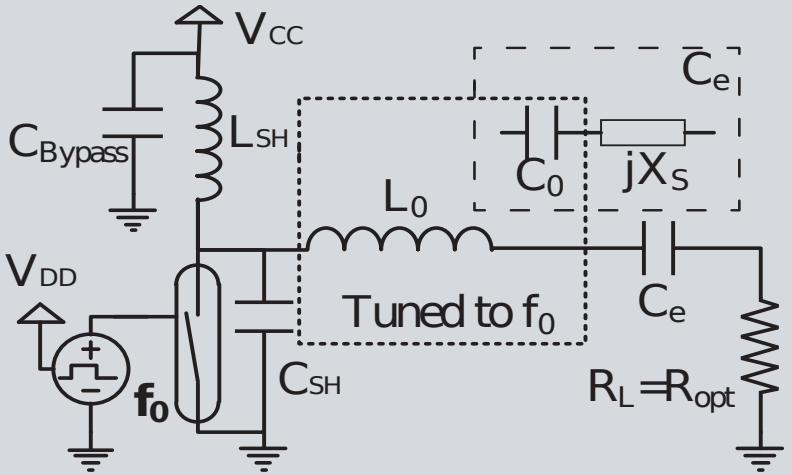
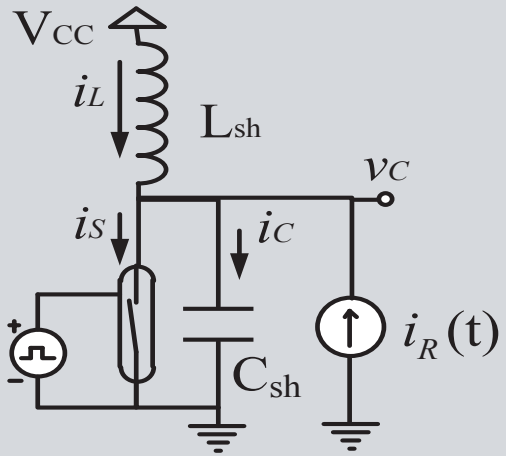
Step 4 - Optimization process

For each circuit, the optimum occurs out of the nominal class-E operation. Therefore, the values computed in the previous steps are the initial point of a optimization process assisted by simulation.

Model of the Class E PA with a finite dc-feed inductance I





$$q = \frac{1}{\omega\sqrt{L_{SH}C_{SH}}} = \frac{\omega_{SH}}{\omega}$$

$$p = \frac{\omega L_{SH} I_P}{V_{CC}} = \frac{Z_{L_{SH}}}{\frac{\sqrt{R_L R_{DC}}}{\sqrt{2}}} = f_1(D,q)$$

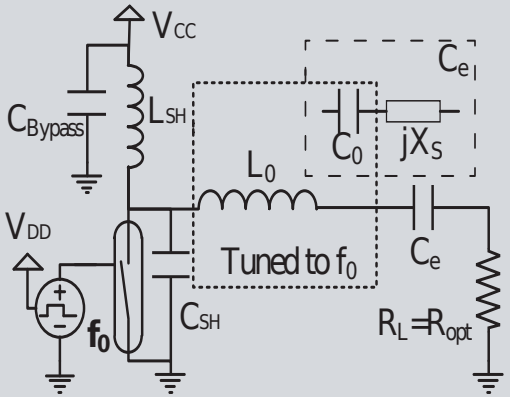
$$i_R(t) = \sqrt{\frac{2P_{OUT}}{R_L}}\sin(2\pi ft + \varphi)\,;\varphi = f_2(D,q)$$

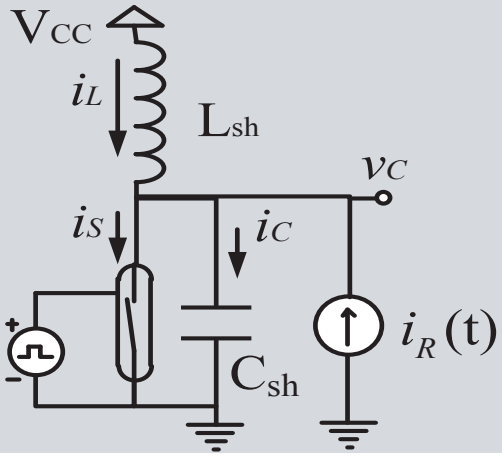
$$Q_L = \frac{\omega L_0}{R_L} = \frac{1}{\omega R_L C_e}$$

ON state $v_{C_{SH\,on}}(t)$ $(0 < t < \frac{2\pi D}{\omega})$

Off state $is_{off} = 0$ $(\frac{2\pi D}{\omega} < t < \frac{2\pi}{\omega})$

Model of the Class E PA with a finite dc-feed inductance II





Switch ON state $v_{C_{SH\,on}}(t)$ $(0 < t < \frac{2\pi D}{\omega})$

$$i_{C_{SH\,on}}(t) = 0$$

$$i_{L_{SH\,on}}(t) = \frac{V_{CC}}{L_{SH}}t - I_P sin(\varphi)$$

$$i_{S\,on}(t) = \frac{V_{CC}}{L_{SH}}t + I_P\left(sin(\omega t + \varphi) - sin(\varphi)\right)$$

Switch Off state $is_{off} = 0$ $(\frac{2\pi D}{\omega} < t < \frac{2\pi}{\omega})$

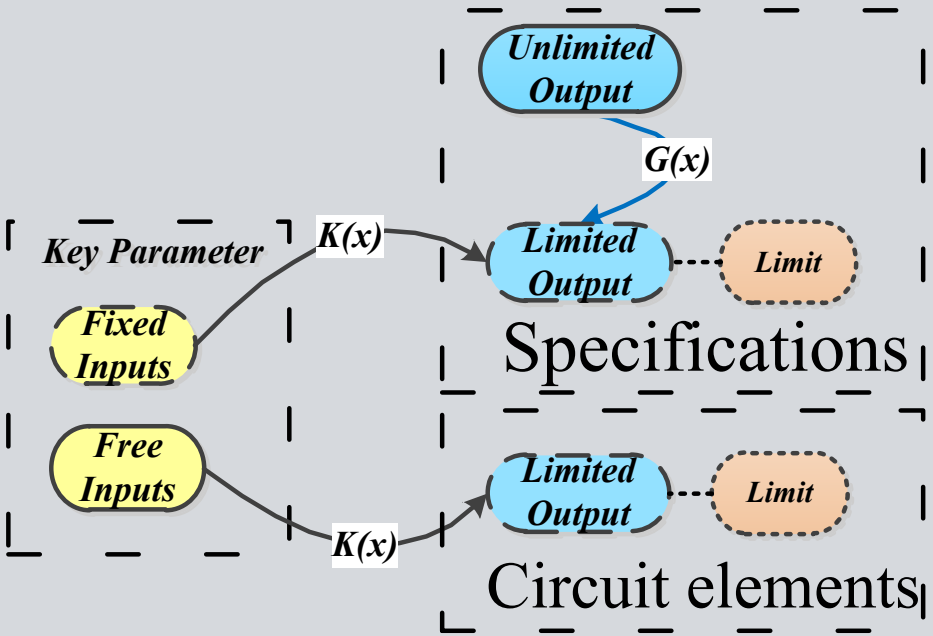
$$i_{C_{SH\,off}}(t) = \frac{V_{CC}}{L_{SH}}t - \frac{1}{L_{SH}}\int_{\frac{2\pi D}{\omega}}^{t} v_{C_{SH}}(\tau)d\tau + I_P\left(sin(\omega t + \varphi) - sin(\varphi)\right)$$

$$i_{L_{SH\,off}}(t) = \frac{V_{CC}}{L_{SH}}t - \frac{1}{L_{SH}}\int_{\frac{2\pi D}{\omega}}^{t} v_{C_{SH}}(\tau)d\tau - I_P sin(\varphi)$$

$$v_{C_{SH\,off}}(t) = V_{CC} + C_1\cos(q\omega t) + C_2\sin(q\omega t) - \frac{q^2}{1-q^2}pV_{CC}\cos(\omega t + \varphi)$$

Proposed design set I

The relations between the input parameters, the circuit element values, and the circuit specification should be known for calculating the PA design space.

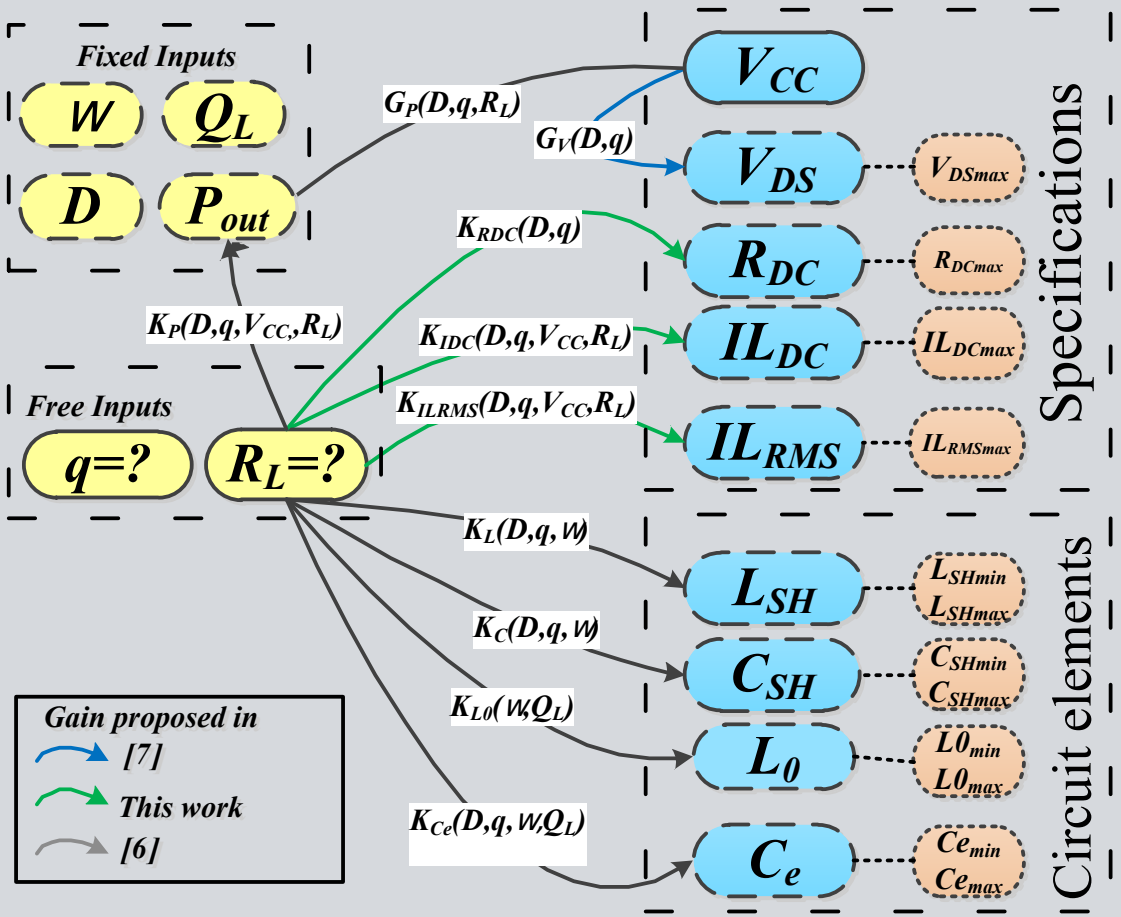


These relations are referred as the design set in [6] and [7].

[6] M. Acar, A. Annema, and B. Nauta, "Generalized design equations for class-e power amplifiers with finite dc feed inductance", in *36th European Microwave Conference*, 2006, pp. 1308–1311.

[7] A. Fajardo and F. Rangel de Sousa, "Simple expression for estimating the switch peak voltage on the class-e amplifier with finite dc-feed inductance", in *2016 IEEE Latin American Symposium on Circuits and Systems (LASCAS)*, 2016.

Proposed design set II



Proposed design set IV

All of these gains are analytic functions of the input variables, therefore the design set can be implemented in any math software for analyzing all the involved trade-offs in the design space.

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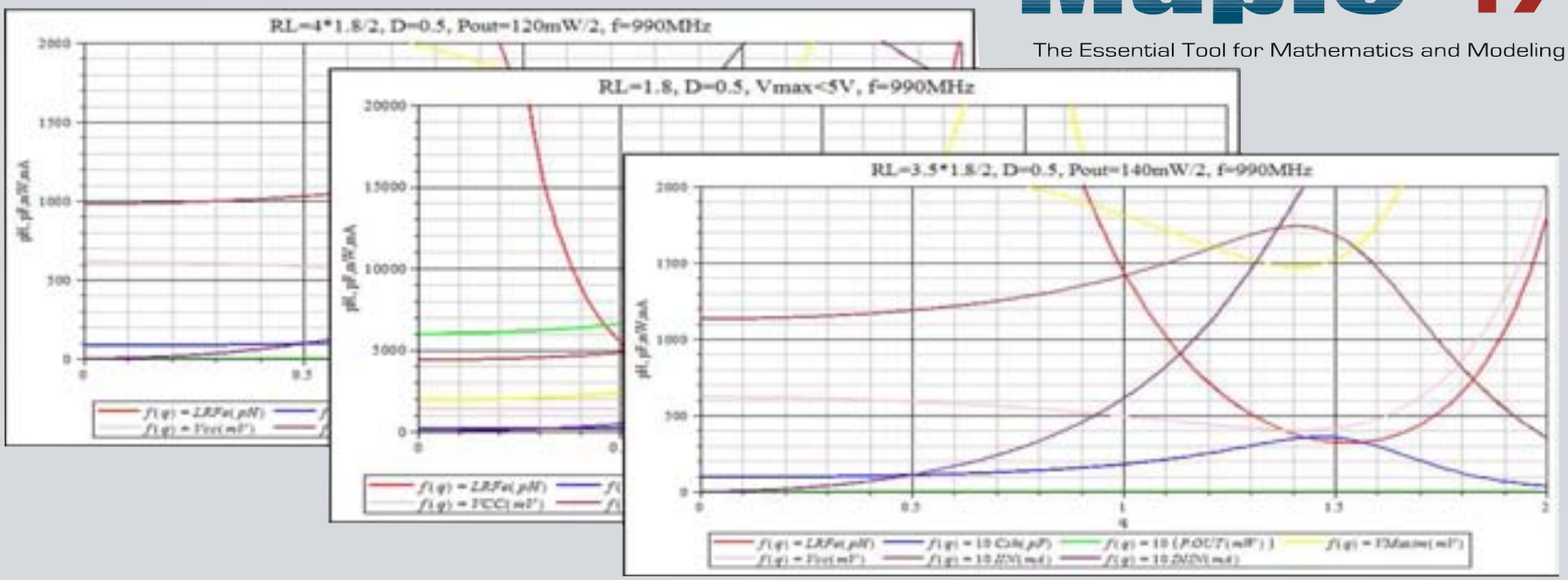
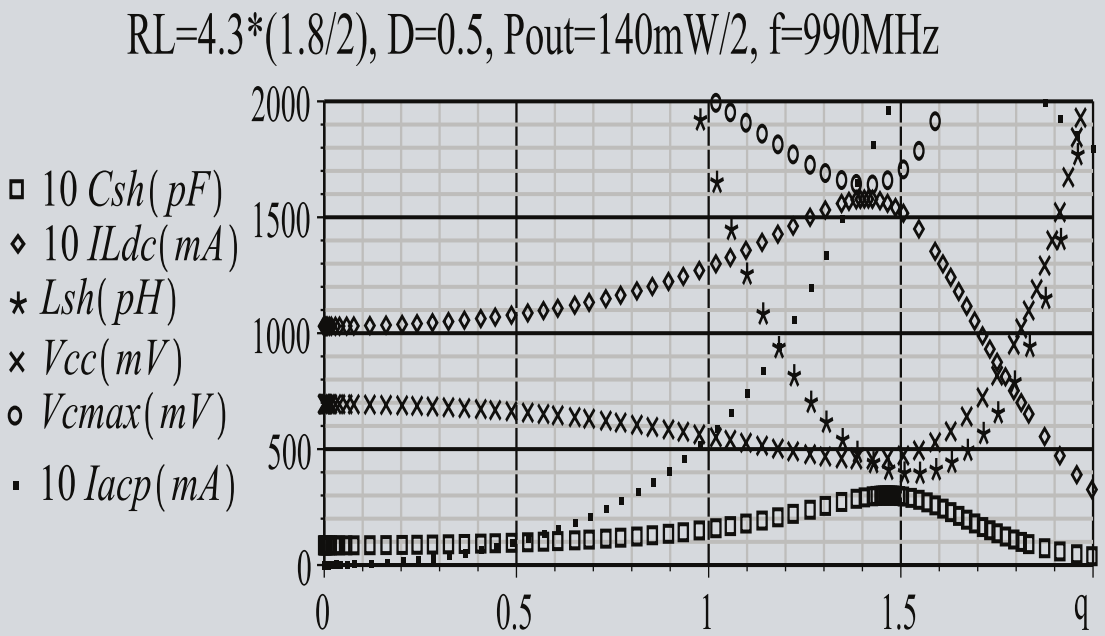


Study Case. Step 1 - Calculate Design space

Sweeps of R_L and q were made. Using:

P_rated	f	P_out	D	q
20 dBm	990 MHz	$0.7 * P\_rated$	50%	< 2



All the goals are simultaneously achieved ($1 < q < 1.1$).

$q = 1.1$, I_{DC} limited (150 mA)
$q = 1$, L_{SH} and $V_{DS_{max}}$ limited (2 nH and 2 V).
The q chosen was 1.05.

Modeling losses and sizing the transistors

Assuming ideal waveforms and modeling M as ideal switch and R_{on}, and L_{SH} as an ideal inductor R_{SH}:

$$P_{Loss} = P_{L_{SH}} + P_{R_{on}} + P_{driver} = {i_{L_{rms}}}^2 R_{SH} + {i_{S_{rms}}}^2 \frac{b}{W} + {V_{DD}}^2 f \alpha a W;$$

Where, a and b are technology parameters [8], the factor α represents the capacitance excess due to the driver implementation. The transistor width that minimize P_{Loss} is:

$$W_{opt} = \frac{\sqrt{a/b}}{V_{DD}} \sqrt{\int_0^{\frac{1}{f}} i_s(t)^2 dt} = \frac{g(D,q)}{1\Big/\sqrt{h(D,q)}} \frac{2V_{CC}\sqrt{\frac{b}{\alpha a \omega}}}{R_L V_{DD}}$$

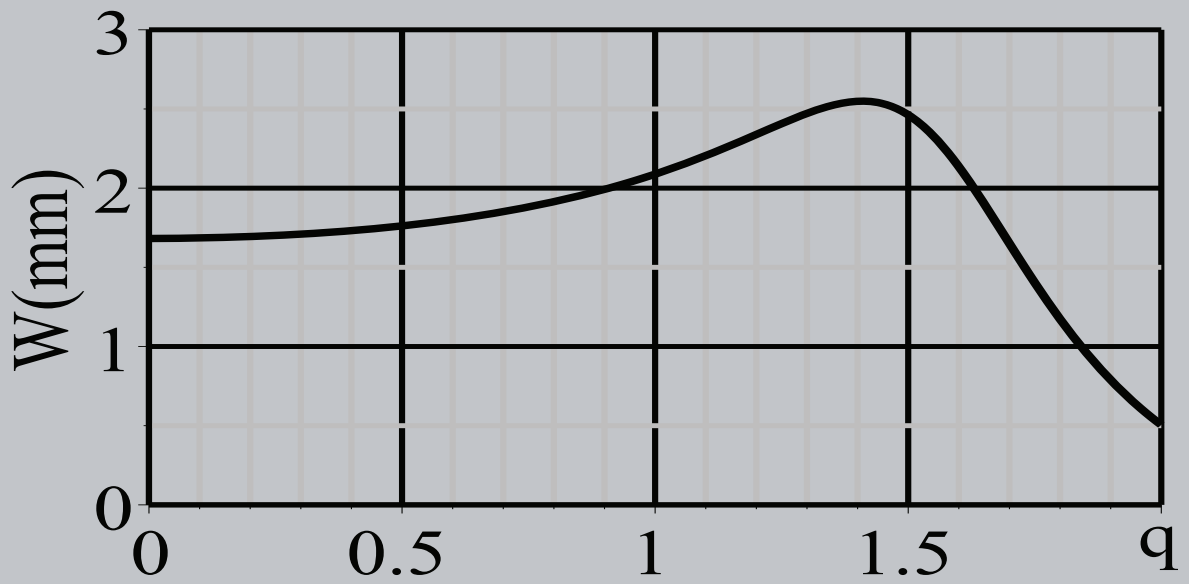
W_{opt} solves the trade-off between the ON-resistance and the gate capacitance. Therefore, sizing M as $W = W_{opt}$ and $L = Lmin = 180nm$ the PAE is maximized.

[8] B. R. W. Stratakos Anthony J. and S. R. Sanders, "High-efficiency low-voltage dc-dc conversion for portable applications.", in *Proc. Int. Workshop on Low-Power Design*, Napa, CA. 1994, pp. 21–27.

Study Case

Step 2 - Estimate the transistor width

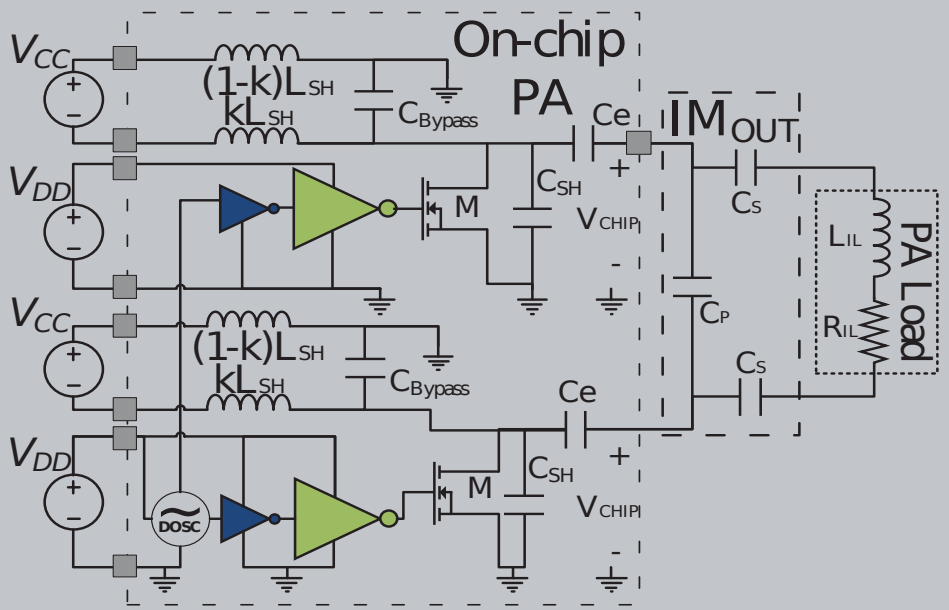
The parameters a and b were estimated by simulation using the MOSFET model in Cadence Design Kit of the used technology ($b = 4.3\text{m}\ \Omega\cdot$ m, $a = 7.8$ nF/m). In the Figure is shown W optimum as a q function, for $D = 50\%$, $R_L = 3.87\ \Omega$, $\alpha = 1.5$ and $P_{out} = 140/2$ mW.

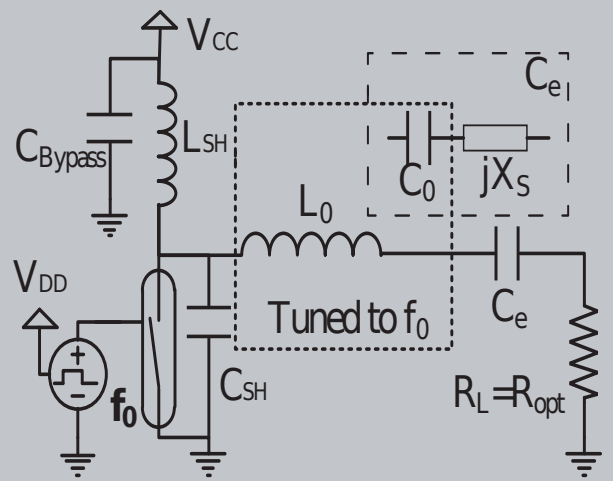


PA Design Methodology

Step 3 - Calculate the matching networks

Calculate the matching networks (IM_{OUT}). The capacitors C_S and C_P form IM_{OUT} that transforms R_{IL} and L_{IL} in R_{opt} and L_0 respectively. C_e combines the impedance jX_s and C_0 at the operation frequency.

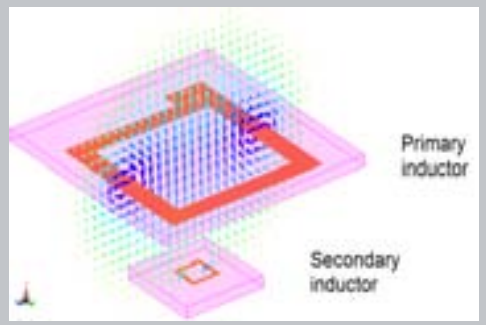


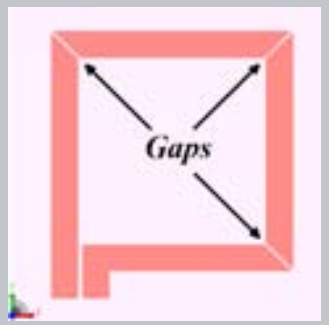


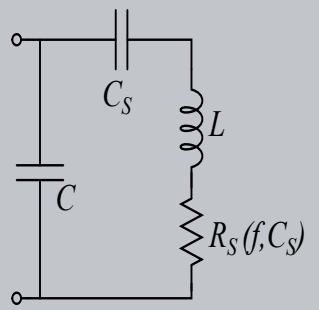
Study Case I

Step 3 - Calculate the matching networks

The IM_{OUT} circuit topology was chosen because it allows to extend the operating frequency of the link when is implemented using a segmented inductor as primary in the inductive link [9][a].







[a] F. L. Cabrera, R. S. Feitoza, and F. R. de Sousa, "Extending the inductor operating frequency for optimally-coupled wireless power transfer systems", in *Microwave and Optoelectronics Conference (IMOC), 2015 SBMO/IEEE MTT-S International*, 2015, pp. 1–5.

Study Case I

Step 4 - Optimization process

In the available design kit the models of the passive elements do not allow automation, therefore a suboptimal optimization was made, where parametric sweeps of some circuit values were used to find the local maximums of the goal function. These sweeps were performed in a predefined order with the available variables, e.g. in post-layout optimization only V_{CC} and the off-chip component values are available.

Study Case II

Step 4- Table of the optimization goals

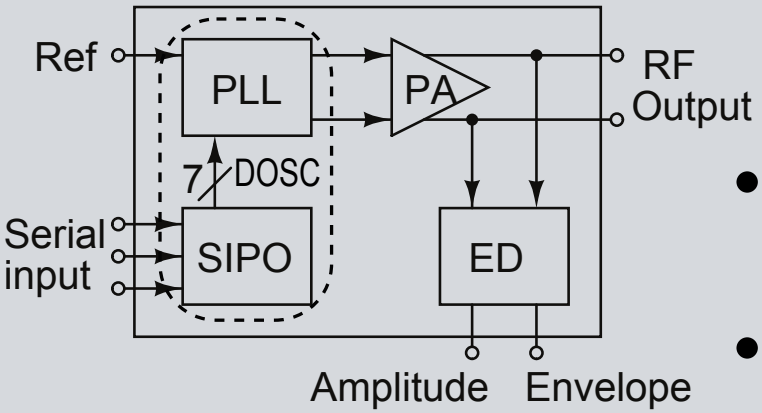
Name	P_L (mW)	η (%)	PAE (%)	R_{DC} W	V_{max} (mV)	$I_{L_{DC}}$ (mA)	R_L type
Ideal	148	99,9	99,9	3,89	2017	137	Ropt
Integrated Lsh	120	86,4	86,4	4,13	1833	129	Ropt
Integrated Csh	138	97,0	97,0	4,03	2063	133	Ropt
Int. MOS W	100	84,2	74,1	4,82	1662	111	Ropt
Int. L,C and M	80	72,1	55,3	5,13	1683	104	LI+IM
Int. L,C and M Opt.	106	73,0	61,5	4,98	1886	121	LI+IM
Int. (L,C, M, Cx). Opt.	100	66,1	55,3	4,75	1629	126	LI+IM
Int. (L,C, M, Cx). Vsin Opt.	114	62,8	62,3	3,99	1476	150	LI+IM
PreLayout	100,1	63	47,3	4,55	1854	132	LI+IM
PostLayout	83,77	59,8	42,2	5,14	1706	117	LI+IM
PostLayout Opt.	116,3	60,3	46,3	4,52	1659	146	LI+IM
PostLayout Vsin	117,5	59,4	45,7	4,41	1682	150	LI+IM

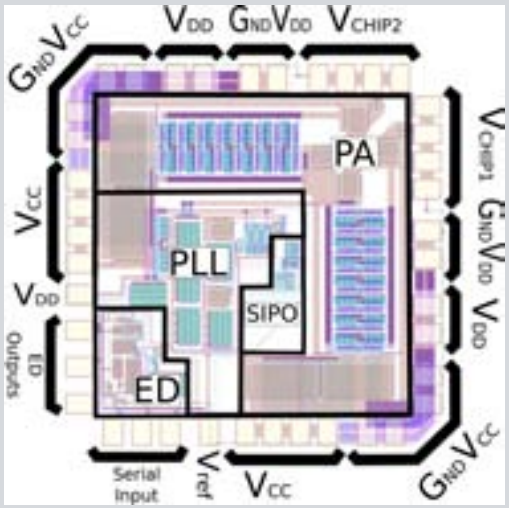
Study Case III

Step 4-Circuit values involved on the optimization process

Name	q	V_{CC} (mV)	(nH)	L_{SH} Q	(pF)	C_{SH} Q	W (mm)	(pF)	C_e Q	C_P (pF)
Ideal	1,05	535	1,5	-	15,7	-	-	7,7	-	-
Integrated Lsh	1,05	535	1,44	17	15,7	-	-	7,7	-	-
Integrated Csh	1,05	535	1,50	-	15,9	98	-	7,7	-	-
Int. MOS W	1,05	535	1,50	-	15,7	-	2,63	7,7	-	-
Int. L,C and M	1,05	535	1,44	17	15,9	98	2,63	6,4	-	6,2
Int. L,C and M Opt.	1,10	600	1,40	17	14,6	105	2,27	6,3	185	6,2
Int. (L,C, M, Cx). Opt.	1,10	600	1,40	17	14,6	105	2,36	6,2	210	6,2
Int. (L,C, M, Cx). Vsin Opt.	1,10	600	1,40	17	14,6	105	3,87	6,2	210	6,2
PreLayout	1,10	600	1,22	15	14,8	57	4,56	6,2	210	6,2
PostLayout	1,10	600	1,22	15	14,8	57	4,56	6,2	210	6,2
PostLayout Opt.	1,10	660	1,22	15	14,8	57	4,56	6,2	210	5,8
PostLayout Vsin	1,10	660	1,22	15	14,8	57	4,56	6,2	210	5,8

CMOS implementation - The CHIP for testing

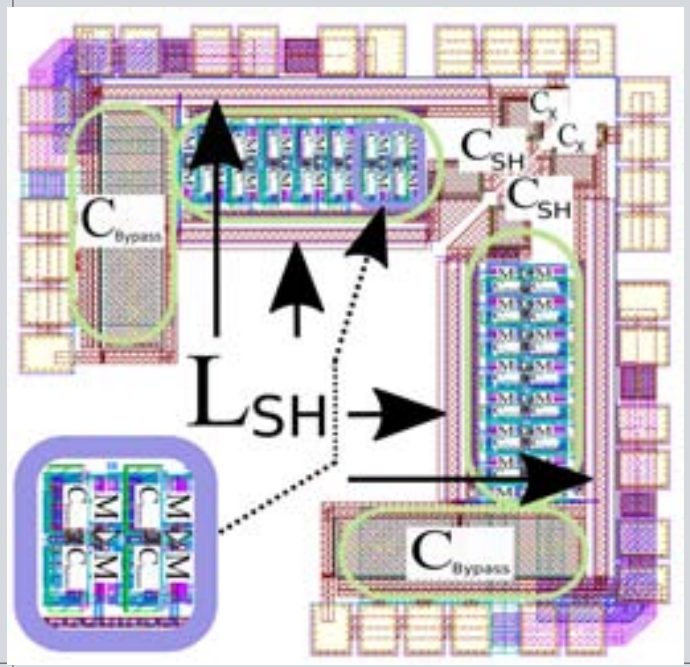


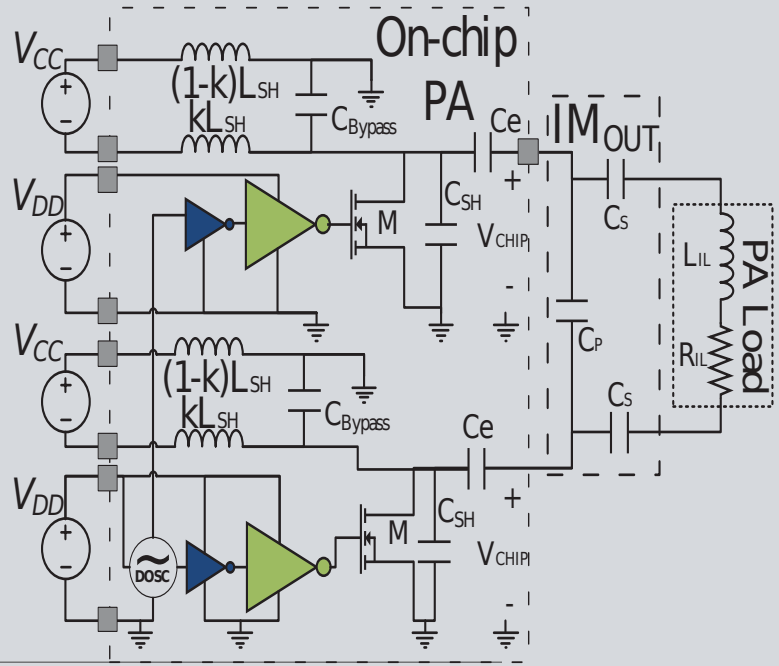


- The PLL generates the V_{AC} using an external signal as reference (Ref).
- The VCO frequency range can be configured using seven control bits by the Serial-Input Parallel-Output (SIPO) interface.
- An envelope-detector (ED) measures the output voltage and the possible response generated by backscattering on the secondary side of the IL.

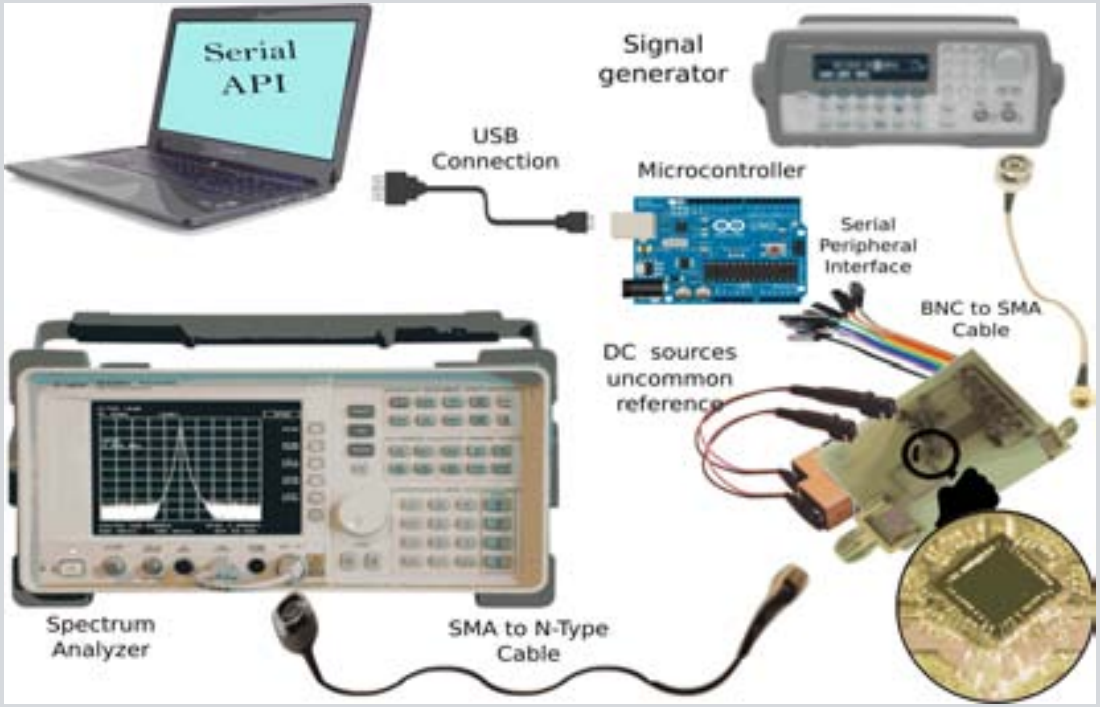
CMOS implementation - PA topology oriented to Layout

Considering the operating conditions imposed by the EPS, the PA specifications and the available technology (i.e., 180nm), a differential class-E PA with split slab inductor was proposed.





On going work...



Conclusions

- An analytic design methodology to find the optimum transistor width of a class-E PA was presented.
- An integrated differential class-E PA with split slab inductor was designed and simulated with good agreement between the initial values of the circuit elements (calculated), and the final values after the optimization process.

Comparison table of the performance

Ref	f (MHz)	P_L (dBm)	PAE %	Area (mm^2)	Tech. (nm)	R_L oms	$L_{DC_{feed}}$ type	PA class	Tested type
2010 [10]	820	29	70,7	0,5	180	50	External	E	Exp.
2016 [2]	990	25,1	58	1,5	180	1,8	w/o L	D	Sim.
This Work	990	20,7	45,7	1,5	180	1,8	On-chip Split L	E	Sim.
2001 [11]	900	29,5	41	4	250	50	Bondwire	E	Exp.
2013 [12]	800	28	40	1,5	180	50	On-chip Transformer	E	Exp.

Acknowledgment

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