Achieving Optimal Efficiency in Energy Transfer to a CMOS Fully-Integrated Wireless Power Receiver

Fabian L. Cabrera and F. Rangel de Sousa, *Senior Member, IEEE*

***Abstract*—This paper presents the design and measurement of an inductive link for transferring energy to a fully-integrated wireless power receiver. The power receiver design was focused on optimizing each factor that contributes to the link efficiency while its size was constrained to 1.5 mm × 1.5 mm in a conventional CMOS 180 nm process. On the power transmitter side, the primary inductor is printed on an FR4 board and its dimensions are selected so as to optimize its quality factor and the magnetic coupling factor. A strategy is proposed to experimentally determine the performance of the entire system. Using the proposed strategy we measured a link efficiency of -25.4 dB at a frequency of 986 MHz, with a primary inductor of average diameter 22 mm and distance 15 mm from the receiver. Considering the characteristics of the receiver: monolithic implementation, chip area, link efficiency and distance to the transmitter, the designed wireless power transfer system exhibits a better performance than state-of-the-art systems.**

***Index Terms*—Body area networks, inductive link, integrated resonator, internet of things, optimal efficiency, wireless power transfer.**

I. Introduction

In the near future billions of devices will be interconnected, enabled by the Internet of Things (IoT) [1]. Several applications are envisaged in different domains including transportation, agriculture, smart homes and healthcare [2]. The transition from idea to reality depends on addressing problems which remain unsolved. As stated in the visionary paper by Mark Weiser [3], *"the most profound technologies are those that disappear"*, however, the physical size as well as the cables used to deliver energy to current IoT-enabled devices are not compatible with the ongoing paradigm shift. Both constraints are related to the method of supplying energy to the devices or how efficient they are in terms of power consumption. Miniaturized embedded systems with wireless communication links are not rare nowadays [4], however they require at least coin-cell batteries, which define the form factor of the IoT device. Considering the healthcare applications, such as body area networks (BAN) [5], [6], several IoT-enabled wearable or implanted devices are foreseen to be carried by a person [7]–[10]. In order for this kind of IoT objects to "*disappear*", they need to have energy autonomy to avoid discomfort on the part of the user. Energy harvesting from the surroundings or wireless power transfer (WPT) are candidates to replace energy carriers in miniaturized circuits. This paper reports measurements obtained on a WPT system including a fully-integrated CMOS batteryless receiver.

Fully-integrated WPT receivers have been proposed applying different strategies [11]–[18]. In [13], the authors describe a UHF radiofrequency identification system (RFID) consisting of a customized reader and a fully-integrated tag designed in a 180 nm CMOS technology. The tag includes an on-chip antenna (OCA), an analog front-end, baseband processing circuits and memory, occupying 0.36 mm^2. The results reported in that work show that the system reading range is 2 mm when the reader output power is 20 dBm. A microsystem for glucose measurement is described in [14]. The sensor electronics are fully integrated in a CMOS 180 nm integrated circuit (IC) with a size of 2 mm^2, including the receiving inductor. The glucose transducer was implemented over the chip top-metal through post-processing techniques. The WPT system operates at 900 MHz and the reading range was 10 mm when 22 dBm was supplied to reading coil. The implementation of functional systems for specific applications has been described in [13], [14]. However, it is not clear whether the energy transmission efficiency was optimized. In [15], the optimization of the efficiency was investigated considering an integrated receiving coil measuring 4.4 mm^2 and designed in a standard 130 nm CMOS process. In the optimization process, the authors fixed the area of the integrated coil and using an iterative procedure they determined the geometry for the transmitter and receiver coils as well as the operating frequency which maximized the efficiency. The system was measured as a two-port network in an on-wafer probe station and the efficiency, estimated from the maximum available gain (MAG), was -18.5 dB when the transmitter and receiver were separated 10 mm. The MAG gives an optimistic result for the efficiency since in a real application lossy devices would be typically used for impedance matching.

In this paper, we describe the design and measurement of a WPT system including a power receiver fully integrated in a 180 nm CMOS process, which was optimized to maximize the energy transfer efficiency. The integrated power receiver comprises an LC resonator, an RF-dc converter, and a power-supply controlled oscillator (PSCO) performing as the system load. This PSCO is used to control a MOS switch operating as a backscattering device. Measuring the frequency of the backscattered signal at the primary side of the link, we

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Fabian L. Cabrera is with the CAE (Computation Applied to Engineering) research group, Federal University of Itajubá - Itabira Campus, MG 35903087 Brazil. (e-mail: fabian@unifei.edu.br).

F. Rangel de Sousa is with Radiofrequency Laboratory, Federal University of Santa Catarina, Florianópolis, SC 88040900 Brazil. (e-mail: rangel@ieee.org).

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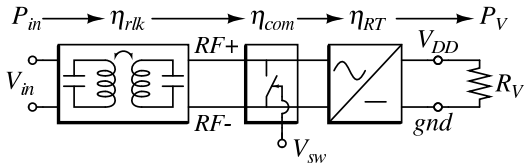


Fig. 1. Typical WPT system with backward communication.

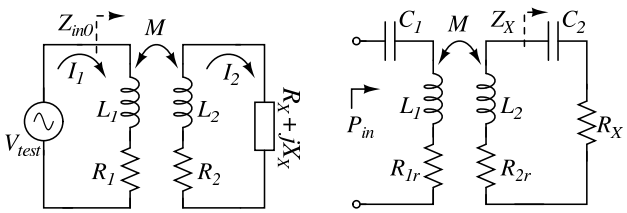


Fig. 2. (a) Inductive link circuit model. (b) Resonant link model.

can estimate the total system efficiency. The integrated LC resonator was wirelessly characterized using a customized method reported in [19]. It resonated at 990 MHz and the quality factor was 21, which is high for a CMOS integrated inductor. Since the link efficiency is proportional to the quality factor of the inductors of the link, the primary inductor also needs to be carefully designed [20]. We designed several primary inductors, each one optimized for different distances from the receiver. We compared our results with state-of-the-art research using a figure of merit proposed by [15] and verified that this system outperforms all other systems, according to published reports, for the scenarios tested. The remainder of this paper is organized as follows: in section II we explain the dependence of the WPT efficiency on the design variables; in section III, the WPT design is described, including the transmitter and receiver parts; the measurement strategy is presented in section IV; the experimental results are reported and discussed in section V. Finally, the conclusions are drawn in section VI.

II. Efficiency of the WPT systems

The efficiency relates to the amount of energy spent on the process of transferring the power extracted from a source to a given load. In the particular case of a WPT system, as illustrated in Fig. 1, this can be formulated as

$$\eta_T = \frac{P_V}{P_{in}}, \tag{1}$$

where P_V is the dc power delivered to the load and P_{in} is the input RF power transferred to a remotely-powered circuit through a resonant inductive link. As depicted in the figure, the WPT total efficiency η_T is affected by three main contributors: a) the resonant link; b) the backscattering modulator; c) the RF-to-dc converter. The resonant link is comprised of a pair of magnetically-coupled resonators and its efficiency is mainly dependent on the inductors geometry and their relative position. A switch is used to modify the impedance of the circuit connected in parallel to the resonant link. The pattern associated with the signal controlling the switch state is perceived in the primary side of the resonant link as amplitude modulation. This technique is best known as backscattering and is very common in passive transponders, especially in RFID tags [21]. Finally, a rectifier performs the conversion of the received RF power into the dc power delivered to the load. Thus, the WPT total efficiency η_T can be rewritten as

$$\eta_T = \eta_{rlk} \cdot \eta_{com} \cdot \eta_{RT}, \tag{2}$$

where

- η_{rlk} is the efficiency of the resonant link;
- η_{com} is a relative measurement of the energy spent during the process of exchanging information with the reader;
- η_{RT} is the RF-to-dc conversion efficiency.

The resonant link and the load modulator are detailed in the next paragraphs. The RF-to-dc conversion efficiency is addressed in section III-A2.

A. Resonant link efficiency

The core of the WPT system is a coupled pair of inductors, as shown in Fig. 2(a), where R_1 and R_2 represent the losses of the inductors L_1 and L_2, respectively. The coupling level of the inductors is measured by the factor k, given by

$$k = \frac{M}{\sqrt{L_1 L_2}}, \tag{3}$$

where M is the mutual inductance. In the figure, $Z_X = R_X + jX_X$ is the equivalent impedance of the circuits loading the link. To devise an expression for the efficiency, we applied straightforward circuit analysis to the circuit of Fig. 2(a). We can calculate the power delivered to the inductive link (P_{in0}=$|I_1|^2 \Re e\{Z_{in0}\}$) and the power received by the load (P_X=$|I_2|^2 R_X$) as follows

$$P_{in0} = |I_1|^2 \left(R_1 + \frac{(\omega M)^2 (R_2 + R_X)}{(\omega L_2 + X_X)^2 + (R_2 + R_X)^2} \right) \tag{4}$$

$$P_X = |I_1|^2 \frac{(\omega M)^2 R_X}{(\omega L_2 + X_X)^2 + (R_2 + R_X)^2}. \tag{5}$$

Then we apply (4) and (5) to find the link efficiency $\eta_0 = P_X / P_{in0}$ resulting in

$$\eta_0 = \frac{(\omega M)^2 R_X}{R_1[(\omega L_2 + X_X)^2 + (R_2 + R_X)^2] + (\omega M)^2 (R_2 + R_X)}. \tag{6}$$

This function is maximized with respect to X_X, when $X_X = -\omega L_2$. Under this condition and using (3), we can rewrite the link efficiency ($\eta_{lk} = \eta_0|_{X_X = -\omega L_2}$) as

$$\eta_{lk} = \frac{1}{\frac{1}{A_0}\left(p_0 + 2 + \frac{1}{p_0}\right) + p_0 + 1}. \tag{7}$$

In (7), $p_0 = R_2 / R_X$, $A_0 = k^2 Q_1 Q_2$, where Q_1 and Q_2 are the quality factors of the primary and secondary inductors, respectively. The resonant condition at the secondary side ($X_X = -\omega L_2$) can be achieved with a series capacitor C_2, as shown in Fig. 2(b). To maximize the power transfer from the source to the link, the inductor L_1 must be resonated by the

capacitor C_1. In practice, C_1 and C_2 have associated losses which are included in R_{1r} and R_{2r}, respectively. Therefore, we can define the primary and secondary resonator quality factors as

$$\frac{1}{Q_{1r}} = \frac{R_{1r}}{\omega L_1} = \frac{1}{Q_1} + \frac{1}{Q_{c1}} \tag{8}$$

$$\frac{1}{Q_{2r}} = \frac{R_{2r}}{\omega L_2} = \frac{1}{Q_2} + \frac{1}{Q_{c2}}, \tag{9}$$

where Q_{c1} and Q_{c2} are the quality factors of C_1 and C_2, respectively. Although series-resonating capacitors are assumed in the model of Fig. 2(b), the expressions obtained in (8) and (9) also apply to parallel-resonating capacitors. By replacing A_0 with $A = k^2 Q_{1r} Q_{2r}$ and p_0 with $p = R_{2r}/R_X$ in (7), η_{lk} becomes η_{rlk} for the resonant link:

$$\eta_{rlk} = \frac{1}{\frac{1}{A}\left(p + 2 + \frac{1}{p}\right) + p + 1}. \tag{10}$$

The value of p that maximizes η_{rlk} can be derived from (10), resulting in

$$p_{opt} = \frac{1}{\sqrt{1+A}}. \tag{11}$$

Equations (10) and (11) can be used with parallel-resonating capacitors by applying the series-to-parallel equivalence of Z_X at a given frequency.

B. Resonant link operating regions

Coupled resonators behave quite differently depending on the level of coupling. In this regard, it is first necessary to define the regions where the coupling is considered to be weak or strong. We depart from the efficiency equation (10) where two asymptotes can be identified depending on the value of A with respect to $1 + \frac{1}{p}$. The resonant link efficiency can be approximated as

$$\eta_{rlk} \approx \begin{cases} \dfrac{A}{\left(p + 2 + \frac{1}{p}\right)} & \text{if } A << 1 + \dfrac{1}{p} \text{ (weak coupling)} \\ \dfrac{1}{p+1} & \text{if } A >> 1 + \dfrac{1}{p} \text{ (strong coupling).} \end{cases} \tag{12}$$

In Fig. 3(a), (12) is plotted as a function of p for several values of A. For higher values of A, the dashed curves approach the solid curve corresponding to the asymptote of strong coupling $\frac{1}{p+1}$. The maximum value for each dashed curve is marked as a circle and corresponds to $p = p_{opt}$ given by (11). When the coupling is weak ($A \to 0$) the p_{opt} value tends to 1, as can be seen in the figure. In this case, the efficiency approaches the first asymptote in (12), wherein the maximum achievable efficiency is $A/4$. As A increases, the p_{opt} value decreases toward 0.

The difference in the behaviors of the two regions is more evident in Fig. 3(b), where efficiency is drawn as a function of A for $p = 1$. In the region of weak coupling the asymptote is $A/4$; therefore, the efficiency is directly proportional to A. For this reason the value of A is the most important variable to maximize in weakly coupled systems, which is the case of most remotely-powered applications. Furthermore, the efficiency is almost independent of A in strong coupling. In the example shown in Fig. 3(b) the efficiency tends to $1/2$.

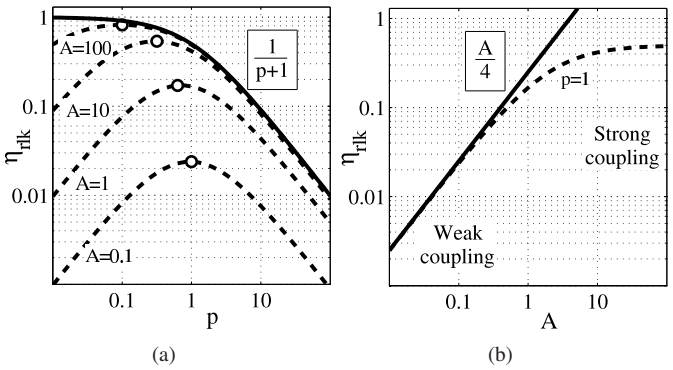


Fig. 3. Resonant link efficiency depending on coupling regions.

C. Energy spent on the backscattering modulation

The backscattering switch in Fig. 1 is controlled by the periodic signal V_{sw}. When the switch is open, all the power received at the secondary side of the resonant link is transferred to the rectifier and in the other case the power is reflected. The effects of backscattering on the efficiency can be analyzed with the aid of the circuit shown in Fig. 4(a). The switching behavior of the system is modeled with S_0 (which does not correspond physically to the switch of Fig. 1), while the voltage source V_0 and the resistor R_0 define the available power. The capacitor C_0 is required to hold the V_{DD} voltage during the time interval in which S_0 is open. In the switching process, the efficiency drop η_{com} is defined as the average power at the load P_V over P_0, which is the power delivered to R_L when S_0 is closed.

The instantaneous power in C_0 and R_V is plotted in Fig. 4(b), assuming a value of C_0 high enough to disregard the voltage ripple in V_{DD}. When S_0 is closed, the power P_0 is decomposed into the capacitor charging power P_1 and the resistor power P_V, thus $P_0 = P_1 + P_V$. When S_0 is open, the net received power is zero. Therefore, the capacitor delivers the power P_V to the load. Based on energy conservation, we

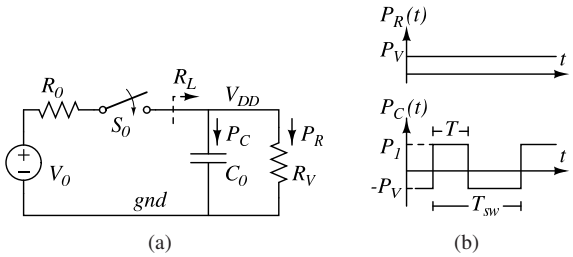


Fig. 4. Switching effect on efficiency. (a) Model. (b) Waves.

can write

$$P_1 T = P_V (T_{sw} - T), \quad \text{thus} \tag{13}$$

$$P_1 = P_V \frac{T_{sw} - T}{T}. \tag{14}$$

In (13), T is the time interval in which S_0 is closed and T_{sw} is the period of the control signal V_{sw}. Using (14) we can calculate η_{com} as

$$\eta_{com} = \frac{T}{T_{sw}} = D, \tag{15}$$

where D is the duty cycle of the control signal. The P_V and P_0 values can be expressed in terms of V_{DD}

$$P_V = \frac{V_{DD}^2}{R_V} \tag{16}$$

$$P_0 = \frac{V_{DD}^2}{R_L}, \tag{17}$$

where R_L is the equivalent resistance seen from the source when S_0 is closed. As $P_V = DP_0$, the relationship between R_V and R_L is obtained as

$$R_L = DR_V. \tag{18}$$

Note that S_0 is put in series with the source to conveniently model the switching behavior of the WPT receiver, but the real switch is connected in parallel to the inductor terminals. Also the parasitics of the switch are not considered in the model of Fig. 4(a). When the switch is open (Fig. 1), the parasitics are formed by a capacitance, that can be added to the resonating capacitor, and a leakage current, that could eventually decrease the resonator quality factor. However, the switch parasitics impact on Q_{2r} was not perceived neither in simulations nor measurements. Another effect of switch parasitics occurs at the transitions between on and off states because of the finite time constant of the circuit. This effect can modify the η_{com} value predicted in (15). Nevertheless, an appropriate selection of the switch dimensions [22] leads to low deviations on η_{com}.

III. WPT System Design

The complete WPT system is shown in Fig. 5, where two main parts can be identified: the transmitter and the receiver. At the transmitter side, the RF source generates the signal at the carrier frequency (f_c), and it is connected to the primary inductor through a capacitive matching network. The capacitive network matches the 50 Ω source impedance to the inductor impedance in order to transfer the maximum power. At the receiver side, the integrated inductor is magnetically coupled to the primary inductor. A resonating capacitor in parallel with the inductor functions as impedance matching. The RF signal at the terminals of the integrated inductor is converted to dc to power the load. The load was designed for the testing of the system: it is a Power-Supply Controlled Oscillator (PSCO), with a frequency (f_{sw}) dependent on the received power. The PSCO output signal controls a switch in parallel with the integrated inductor. The impedance matching blocks are designed to transfer power from the source to the load when the switch is open. On the other hand, when the switch closes, the power destined to the load is reflected

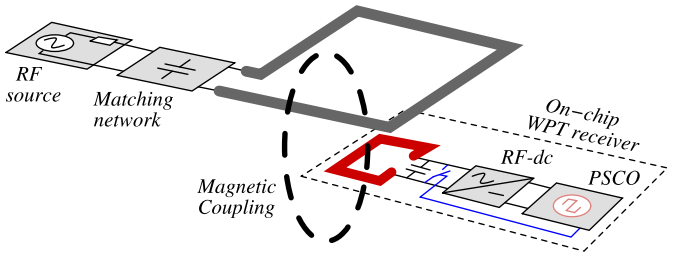


Fig. 5. Wireless power transfer system.

toward the RF source. Thus, the backscattering communication is used to provide information regarding the amount of power received at the load.

Since the received power is estimated from the measured frequency, the sensitivity of the PSCO frequency to power consumption must be stronger than to other variables (such as temperature and process variations). Part of this is accomplished by performing the tests at room temperature and calibrating the measurement with a replica of the oscillator fabricated on the same chip (thus compensating die-to-die process variations).

The WPT design starts from the efficiency equation:

$$\eta_T = \frac{\eta_{com}\eta_{RT}}{\frac{1}{k^2 Q_{1r} Q_{2r}}\left(p + 2 + \frac{1}{p}\right) + p + 1}, \tag{19}$$

which explicitly shows the factors that affect the efficiency and must therefore be optimized. The design variables related to these factors are summarized in Table I, where they are listed in the same order in which they should be designed. Firstly, the duty cycle of the backscattering is chosen to be 50% to guarantee the communication even when the received power is low. Secondly, the Q_{2r} value, and hence Q_2, must be optimized through the appropriate selection of the dimensions of the integrated inductor, as well as its operating frequency. The η_{RT} and the p values are dependent on the rectifier design, the load R_V and the power level P_V, and this needs to be considered in the PSCO design. Finally, the choice of the dimensions of the primary inductor must optimize the k and Q_{1r} values.

TABLE I
Variables involved in the WPT optimal design.

Part	Receiver				Transmitter	
Objectives	η_{com}	Q_{2r}	η_{RT}	p	k	Q_{1r}
Design variables	• Fixed value: 0.5	• Integrated inductor • Frequency (f)	• Rectifier • Load (R_V) • Power (P_V)		• Primary inductor	

A. Receiver

The receiver is constrained to be fully integrated in a CMOS die of 2.25 mm^2 [22]. The design of the receiver building blocks is explained in this section.

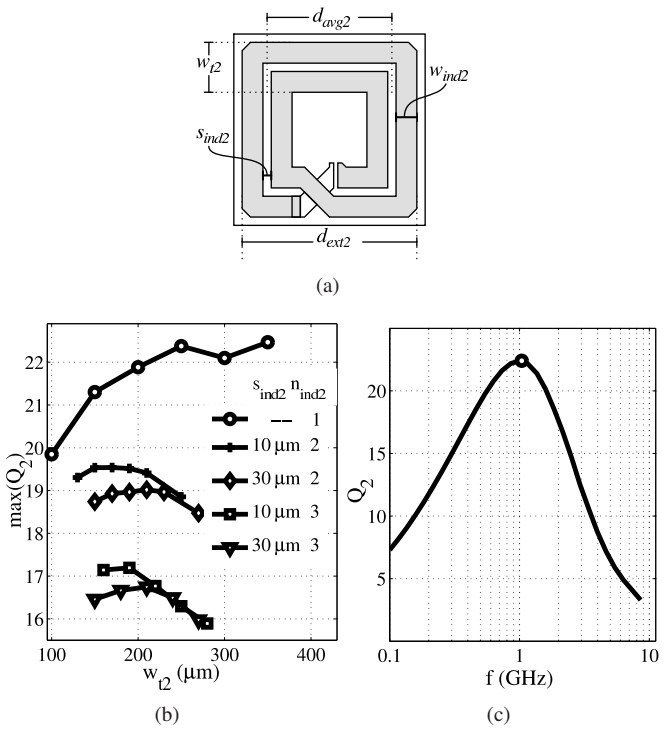


Fig. 6. On-chip inductor: (a) Geometry details of a two-turns inductor. (b) Maximum Q_2 for several inductors as function of the variable w_{t2}. (c) Q_2 of the one-turn inductor when $w_{ind2} = 250\,\mu$m as function of the frequency.

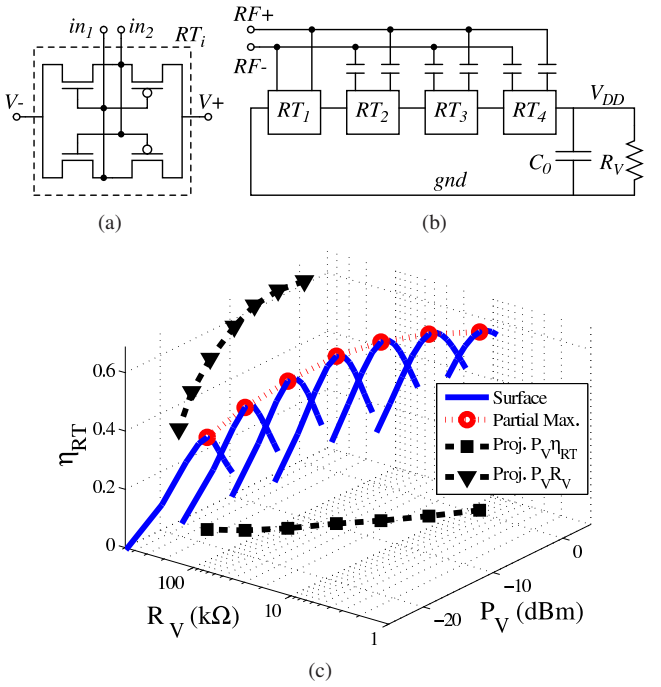


Fig. 7. Rectifier: (a) CMOS schematic of each stage. (b) Block diagram. (c) Simulated efficiency as function of the load R_V and the power delivered to the load P_V.

1) Inductor: The inductor is perhaps the most challenging component in a CMOS integrated WPT receiver, due to its proximity with the lossy substrate and to the fact that it must occupy the outermost area of the chip to maximize the enclosed magnetic flux. The first condition has led to several studies on the optimization of the quality factor of integrated inductors. A widely-accepted technique to improve the quality factor is the use of patterned shields below the inductor. However, this technique cannot be applied to WPT inductors because of the second condition. Since the inductor occupies the outermost area, the remaining circuits must be positioned in the inductor inner area which complicates the fabrication of patterned shields. Moreover, the circuits interfere with the magnetic flux in different levels depending on their layout. This interference is difficult to estimate in simulations because of the complex geometry of the circuits. Our approach to this problem is to design the inductor without considering the interference of the inner circuits and then carefully design the layout to minimize the interference. Guard rings, large area capacitors, and high-count number of pads were avoided to reduce the effects of induced currents loops. Moreover, the power distribution tree was carefully designed for minimizing the interference on the magnetic flux [19].

The variables related to the inductor geometry are shown in Fig. 6(a), as an example of an inductor with 2 turns (n_{ind2}). The inductor is drawn at the top metal of the technology, which is also the thickest (to give the lowest sheet resistance). The external diameter (d_{ext2}) was set to 1460 μm which is the maximum allowed in the constrained area. The average diameter (d_{avg2}) can be computed as $d_{ext2} - w_{t2}$. The quantity w_{t2} was defined as $n_{ind2}w_{ind2} + (n_{ind2} - 1)s_{ind2}$ to better compare the inductors with different n_{ind2}. We swept the linewidth w_{ind2}, the spacing between turns s_{ind2} and n_{ind2} with the aim of finding the best quality factor. Full-wave electromagnetic simulations were carried out using the software EMPRO® for several configurations. The quality factor of each inductor was computed as a function of the frequency and only the maximum values are plotted in Fig. 6(b). Based on this figure, we can conclude that the quality factor decreases as n_{ind2} increases, so the optimum value of n_{ind2} is 1. Also, for the one-turn inductor the maximum quality factor of 22.4 is obtained when w_{ind2} is 250 μm (hence $d_{avg2} = 1210\,\mu$m). This maximum quality factor is achieved at the frequency 1.04 GHz as can be seen in Fig. 6(c). Therefore, this frequency was selected for the operation of the inductive link. Considering that the magnetic coupling factor may be slightly decreased by the selection of large values of w_{ind2}, we preferred the 250 μm-width even though the inductor of 350 μm-width presents a similar quality factor. A dual-MIM capacitor of 11.6 pF was integrated in parallel to the inductor to resonate at the optimum frequency. The layout of the capacitor was optimized in such a way that the resulting value of Q_{2r} was 21.7. The design was verified by measurements as reported in [19].

2) Rectifier: The rectifier topology was based on [23], due to its high efficiency and simplicity, and is shown in Fig. 7(a). Its detailed analysis is out of the scope of this paper and can be found in [23], [24]. The number of stages selected was four, as shown in the block diagram of Fig. 7(b). All transistors in Fig. 7(a) have the minimal length (180 nm) and the width is 30 μm. The NMOS transistors are triple-well devices, and

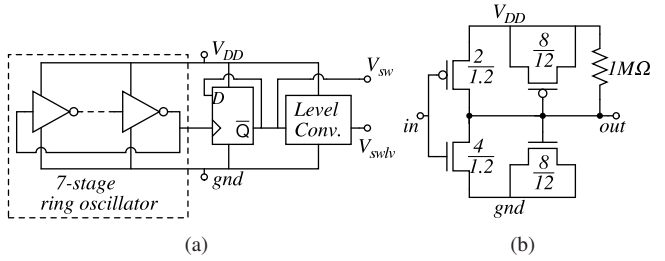
thus their sources can be connected to their body terminals, thereby keeping at minimum the voltage required to turn-on the NMOS transistors. Under these characteristics, the rectifier was simulated in the Cadence® environment, resulting in the efficiency depicted in Fig. 7(c) as a function of R_V and P_V. In the figure, P_V is used instead of the input power of the rectifier (P_{inRT}) to have a visualization reference in common with other figures in the rest of the paper. The relationship between P_V and P_{inRT} is given by

$$P_V = \eta_{RT} \cdot P_{inRT}. \tag{20}$$

The solid curves belong to the surface describing η_{RT}. From the figure we can conclude that for each value of R_V there is a P_V value that maximizes the efficiency $\left(\frac{\partial \eta_{RT}}{\partial P_V} = 0\right)$. These values are marked with circles. When projected onto the $P_V\eta_{RT}$ and $P_V R_V$ planes these points of partial maximum form the dashed curves of Fig. 7(c). In the projection onto $P_V\eta_{RT}$ we can see that η_{RT} is greater than 45% for P_V ranging between -20 dBm and 0 dBm, which is advantageous because it means that the system can operate within a wide range of power levels. However, to achieve these levels, it is necessary to follow the curve of the partial maximum points. This condition can be achieved by designing the load so that the relationship between R_V and P_V is as indicated in the projection $P_V R_V$ of Fig. 7(c), which was the motivation for designing a variable load as shown below.

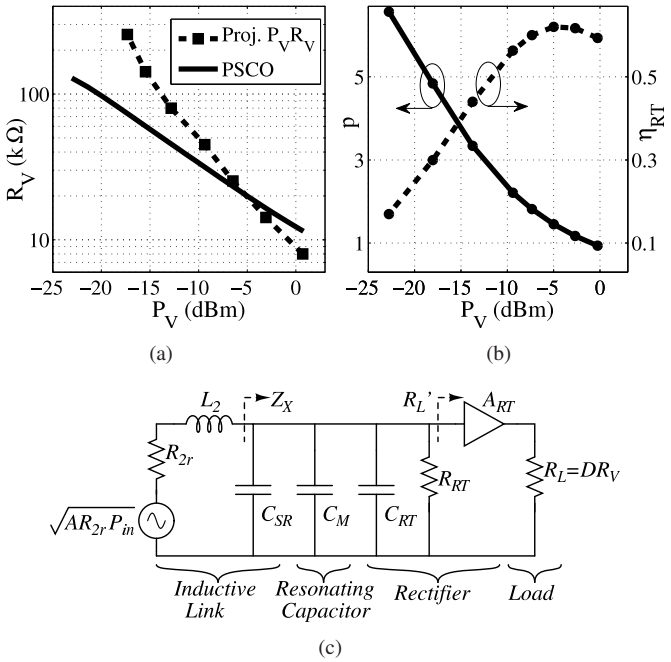
3) Variable load: A PSCO is suitable to convert the amount of received power into a frequency quantity. Moreover, the PSCO consumption is a function of V_{DD}, thus its equivalent load R_V can be adjusted to the desired curve described in the previous paragraph. The PSCO is based on a seven-stage ring oscillator, as shown in Fig. 8(a). A frequency divider based on a flip-flop is used after the oscillator to guarantee a duty cycle of 50%. The output signal V_{sw} controls the switch responsible for the backscattering response. The level converter block generates the V_{swlv} signal to drive the 1.8 V NMOS switches, while V_{sw} can vary between 0 V and 3.6 V. The schematic of the inverter used in the oscillator is shown in Fig. 8(b). In addition to the NMOS and PMOS transistors forming a conventional inverter, we added transistors with the sources connected to the drains acting as capacitors to decrease the oscillation frequency. We also added a 1 MΩ resistance in parallel with the PMOS transistor to allow the circuit operation at low V_{DD} values. Thus, the designed circuit can operate for V_{DD} between 0.7 V and 3.6 V, as verified in simulations with typical-case models.

The dimensions of the transistors of Fig. 8(b) are shown in μm. These values were selected to approximate the P_V-R_V relationship of the PSCO to that desired according to the projection in Fig. 7(c). The two curves are compared in Fig. 9(a), where they exhibit similar behavior, although they do not overlap. The R_V value decreases when V_{DD}, and hence P_V, increases. The average current consumed by the PSCO rises for two reasons: the increase in the drain and gate transistor voltages, and the increase in the oscillation frequency f_{sw}. The rectifier efficiency is shown in Fig. 9(b). This curve was obtained from post-layout simulations of the WPT receiver



(a) (b)

Fig. 8. Power-supply controlled oscillator: (a) Block diagram. (b) Inverter (width and length of transistors are in μm).



(a) (b)

(c)

Fig. 9. Variable load characteristics: (a) R_V curve. (b) Efficiency and p curves. (c) Circuit model for the impedance transformation.

including the PSCO designed herein. Due to the variable load profile, the rectifier efficiency is kept at close to 60% for P_V ranging from -10 dBm to 0 dBm. Moreover, the rectifier operates with reasonable efficiency over a wider P_V range.

The maximum value of η_{RT} is observed when P_V is close to -5 dBm. The location of this maximum is directly related to the choice of 30 μm for the rectifier transistors width (Fig. 7(a)). This choice is appropiate in this case because the maximum η_{RT} lies in the same region in which p approaches 1, which is its optimum value in weak coupling. The simulated p values are plotted in Fig. 9(b) as a function of P_V. The circuit in Fig. 9(c) helps us to understand how R_V is transformed into R_X ($\Re e\{Z_X\}$). The voltage source is the equivalent of the primary side when the link is weakly coupled. In the figure, C_{SR} models the self-resonant frequency of the inductor, C_M is the dual-MIM capacitor and C_{RT} is the input capacitance of the rectifier. The resistor R_{RT} accounts for the losses on the rectifier. The voltage gain at the rectifier is modeled with A_{RT}. The output current is reduced by A_{RT} because there is no power gain. Consequently, the resistance R_L is reduced by the rectifier to ${R_L}' = R_L/A_{RT}$.

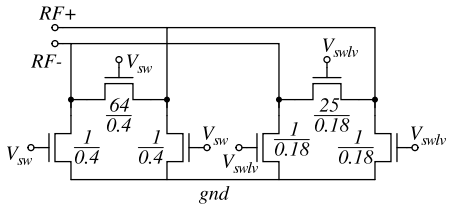


Fig. 10. Switch for load modulation (width and length of transistors are in μm).

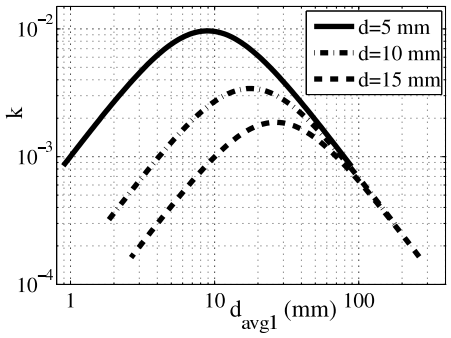


Fig. 11. Magnetic coupling factor when the secondary (integrated) inductor has $d_{avg2} = 1210\,\mu$m.

4) Backscattering device: The switch used for the load modulation is implemented as shown in Fig. 10. Two NMOS transistors (a thin-oxide NMOS controlled by the 1.8 V signal and a thick-oxide NMOS controlled by the 3.3 V signal) are connected between the terminals of the inductor. Their lengths were kept at the respective minimum values to decrease the ON resistance, while their widths were designed to keep the ON-OFF amplitude ratio higher than 10. Other transistors were used to tie RF+ and RF- down to ground, aiming to decrease the ON resistance of the main switches.

B. Transmitter

Equation (19) shows that the link efficiency is dependent on the inductor (resonator) quality factors, the magnetic coupling factor and the impedance matching conditions. Thus, the design of the WPT receiver included the optimization of Q_2 (Q_{2r}) and p. Also, the value of k was partially optimized by selecting the largest diameter possible for the integrated inductor in the available chip area. Therefore, the primary inductor design must optimize Q_1 (Q_{1r}) and k. Since the value of k is strongly dependent on the distance between the inductors (d), this parameter must be considered for the sizing of the transmitter. This can be observed, for instance, in Fig. 11, where the value of k is plotted as a function of the primary inductor average diameter (d_{avg1}) for three different distances. The dimensions of the inductor designed in section III-A1 are used to obtain the k values of Fig. 11. In each curve we can identify a peak occurring at different values of d_{avg1}. Based on the figure we can infer that the optimal value of d_{avg1} increases with the distance.

In order to demonstrate the functionality of the integrated WPT receiver we designed four different printed inductors, as shown in Fig. 12. Their main characteristics are summarized in Table II. Each inductor is designed for a nominal distance d_{nom}, however it can be used at different distances. The inductor (a) is designed for the strong-coupling test. Strong coupling is ensured by placing the WPT receiver in the same plane as the transmitter ($d_{nom} = 0$), as can be seen in Fig. 12(a). Also, the dimensions of the inductor are such that the inner area is slightly larger than the chip, resulting in a simulated k value of 0.3. When the inductor (a) and the WPT receiver are placed together, the input impedance matches the 50 Ω measurement system without any matching network.

The optimal value of d_{avg1} is 8 mm for a 5 mm distance, as observed in Fig. 11. Two versions of this transmitter inductor were fabricated. In the first, two capacitors of the matching network are implemented with varactor diodes allowing fine tuning of the real and imaginary parts of the input impedance. The small signal quality factor of the varactor varies between 75 and 300 depending on the bias voltage. The simulated inductor quality factor is 280, which means that the varactor quality factor has a significant effect on Q_{1r}. This issue is even more relevant for high input power because of the non-linearity of the diodes. That is why we implemented the inductor of

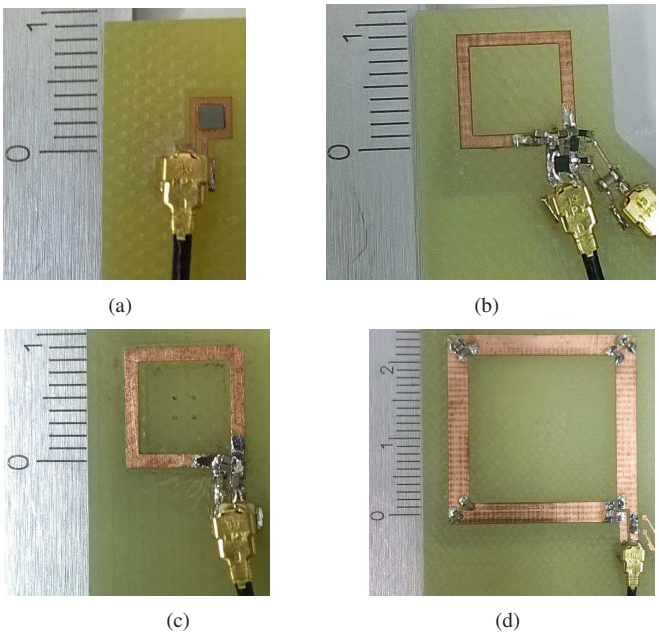


Fig. 12. Transmitter inductors: (a) $d_{avg1} = 2.4$ mm. (b) $d_{avg1} = 8$ mm matched with varactors. (c) $d_{avg1} = 8$ mm without varactors. (d) $d_{avg1} = 22$ mm.

TABLE II
SUMMARY OF DESIGNED TRANSMITTER INDUCTORS.

Inductor	d_{avg1} (mm)	w_{ind1} (mm)	Q_{1r} (Meas.)	d_{nom} (mm)	k @ d_{nom} (Sim.)	Coupling @ d_{nom}
(a)	2.4	0.6	80	0	0.3	strong
(b)	8	1	–	5	0.01	weak
(c)	8	1	147	5	0.01	weak
(d)	22	2.8	141	15	0.002	weak

Fig 12(c), wherein the impedance matching network consists of capacitors with fixed values but high quality factors (around 600, according to the manufacturer).

For a distance of 15 mm we chose a d_{avg1} value of 22 mm based on the dashed curve of Fig. 11. However, the selfresonant frequency of this inductor is around 1 GHz, so its original structure can not be used to operate with the designed WPT receiver. To overcome this problem, the inductor was divided into four-segments [25], as shown in Fig. 12(d). The quality factors of the resonators formed by the inductors (c) and (d) were measured using the contactless method proposed in [19]. This method can not be applied to the resonator with the inductor (b) because of the non-linearity of the varactors. The Q_{1r} value for inductor (a) was measured directly with a vector network analyzer.

IV. Measurement Strategy

To devise a measurement strategy, it is convenient to develop a behavioral model of the system considering its linear time-variant (LTV) characteristic. Firstly, the inductive link is replaced with a linear two-port box, with a power source connected to the input port as shown in Fig. 13(a). At the output port, two impedances are switched as a function of the signal generated by the receiver oscillator, providing the time-variant behavior. The switching impedance operation can be represented by multiplication using a squared signal. So that, from the source, the circuit of Fig. 13(a) can be transformed into the model of Fig. 13(b), where the reflected and transmitted signals are separated on different paths. The reflected signal measured at the transmitter side may be written as:

$$V_r(t) = \alpha_1\alpha_2 V_c(t) V_{sw}(t); \tag{21}$$

where:

$$V_c(t) = A_c \cos\omega_c t; \tag{22}$$

$$V_{sw}(t) = B_0 + B_1 \cos\omega_{sw} t + B_3 \cos 3\omega_{sw} t + \cdots \tag{23}$$

If we consider only the first two terms of the series in (23) then $V_r(t)$ can be rewritten as:

$$V_r(t) = \alpha_2\alpha_2 A_c \left[B_0 \cos\omega_c t + \frac{B_1}{2} \cos(\omega_c \pm \omega_{sw}) t \right]. \tag{24}$$

According to (24) the reflected signal is mainly composed of three tones: one at the carrier frequency and the other two located at each side of the carrier. Since the information on the power level received by the transponder is contained in the value of f_{sw}, we can extract it from the separation of the lateral tones from the center carrier in the frequency domain.

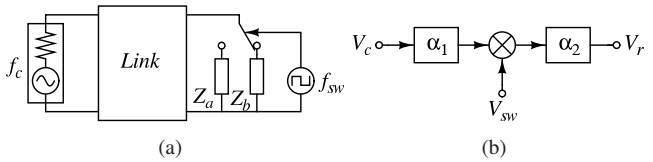


Fig. 13. Backscattering model: (a) Block diagram. (b) Signal flow diagram.

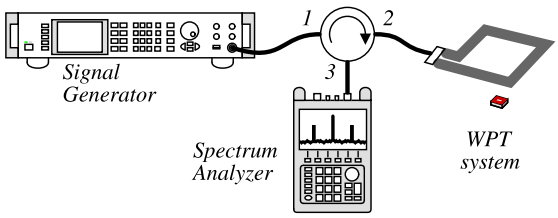


Fig. 14. Test setup for WPT system.

This can be carried out using the configuration shown in Fig. 14. The R&S® SMA100A signal generator serves as an RF source with a power capability of up to 26 dBm. It is connected to a circulator which separates the transmitted signal (from port 1 to port 2) from the reflected signal (from port 2 to port 3). The WPT system is then connected at port 2 of the circulator. On the other hand, the reflected signal can be measured at port 3 of the circulator with an Agilent® N9913A spectrum analyzer.

The frequency f_{sw} is a function h of the power received by the variable load (P_V). Assuming that h is a one-to-one function, we can express the value of P_V as:

$$P_V = h^{-1}(f_{sw}), \tag{25}$$

where h^{-1} is the inverse function of h. The function h can be experimentally obtained from an on-chip characterization of the variable load. By knowing h, we can measure the total efficiency as:

$$\eta_T = \frac{P_V}{P_{in}} = \frac{h^{-1}(f_{sw})}{P_{in}}, \tag{26}$$

where P_{in} is the input power of the WPT system. The losses associated with the cables, transitions and circulator can be deducted from the measurement by executing a careful calibration.

An example of the reflected signal spectrum (S_r) can be seen in Fig. 15, which corresponds to a measurement with $d = 10$ mm and $d_{avg1} = 22$ mm when the input power is 21 dBm. In the figure we can see the carrier at the center frequency (986 MHz) and the two side tones separated by around 3.6 MHz from the carrier, therefore $f_{sw} = 3.6$ MHz. From the measurement of the PSCO we found that the power consumed P_V is -5.1 dBm when the oscillation frequency is 3.6MHz. Thus, we can conclude that the total efficiency is -26.1 dB for the WPT system tested under these conditions.

V. Experimental Results and Discussion

In this section, we present the measurement results of the WPT system to determine its total efficiency. Photographs of the WPT system and the integrated receiver can be seen in Fig. 16. As a first step, a contactless method for testing the integrated LC resonator characteristics was proposed [19]. The Q_{2r} value measured was 20.8 at the resonance frequency of 0.99 GHz. The transmitter inductors were thus designed to operate at this frequency and the experiments were performed as explained below.

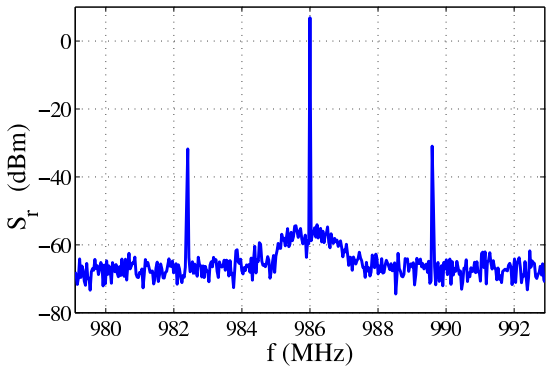
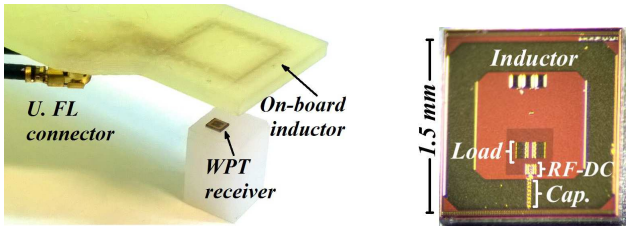
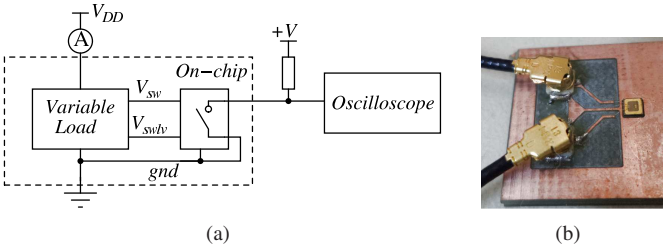


Fig. 15. Spectrum of the reflected signal measured when $d = 10$ mm, $d_{avg1} = 22$ mm and the input power is 21 dBm.



(a) (b)

Fig. 16. WPT system test: (a) Photograph. (b) Receiver in detail.



(a) (b)

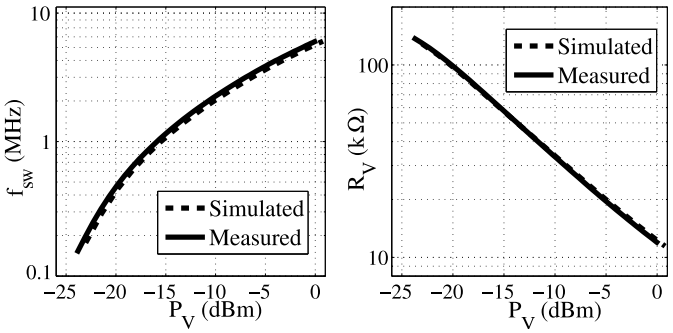
Fig. 17. Variable load characterization: (a) Test setup. (b) Photograph.

A. Variable Load Characterization

A replica of the variable load was included in the chip, so that the relationship between the oscillation frequency (f_{sw}) and the power consumed by the load (P_V) could be measured. A diagram of the test setup and a photograph of the variable load characterization are shown in Fig. 17. The experimental results are compared with the simulations in Fig. 18, the oscillation frequency is shown in Fig. 18(a) and the equivalent resistance (R_V) of the variable load circuit is plotted in Fig. 18(b). The frequency of the oscillator varies from 150 kHz to 5.5 MHz when its power consumption varies from -24 dBm to 0 dBm. In the same frequency range, the equivalent resistance varied from 130 kΩ to 12 kΩ. These results allow us estimate the overall efficiency of the system with the aid of (26).

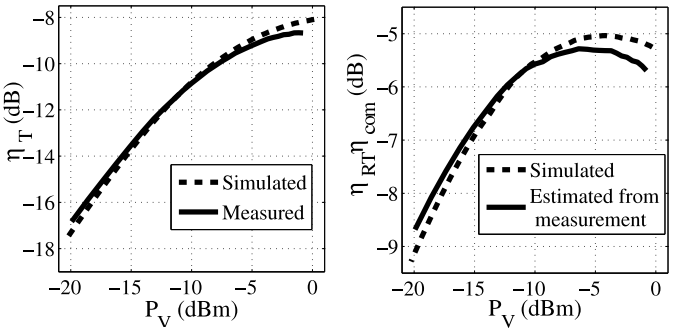
B. Test under the strong-coupling regime

Using the transmitter inductor of Fig. 12(a) and the method described in the previous section, we obtained experimentally η_T, as plotted in Fig. 19(a). The A value is around 150 for



(a) (b)

Fig. 18. PSCO results: (a) Oscillation frequency. (b) Equivalent resistance.



(a) (b)

Fig. 19. (a) Total efficiency under strong coupling regime. (b) Combined efficiency of the rectifier and the communication.

this setup, so the link operates in the strong-coupling regime. According to (12) the resonant link efficiency in this regime is only dependent on p, thus we can estimate $\eta_{RT}\eta_{com}$ from the multiplication of η_T by $(p+1)$, resulting in the solid curve of Fig. 19(b). The p value used for this calculation is the same as that in Fig. 9(b).

C. Sensitivity of the efficiency to the frequency

The primary inductor matched with the varactors (Fig. 12(b)) was used to explore the WPT efficiency while sweeping the carrier frequency. The test was performed with $d = 1$ mm and the input power was kept at a constant value of 0 dBm, resulting in the curve shown in Fig. 20. The efficiency presents a maximum value of -16.3 dB at 986 MHz and decreases by less than 0.2 dB (5%) in a ±5 MHz band.

D. Dependence of efficiency on the distance

The experimental verification of the efficiency was also carried out for several distances between the transmitter and the WPT receiver, as shown in Fig. 16(a). The chip was placed over a Teflon surface, which provides low interference with the electric and magnetic fields. The transmitter was then positioned at the desired distance with the help of a CNC (computer numerical control) positioning machine. Figures 21(a) and 21(b) show plots of the results obtained when the transmitter inductor has d_{avg1} values of 8 mm (Fig. 12(c)) and 22 mm (Fig. 12(d)), respectively. The efficiency is greater in

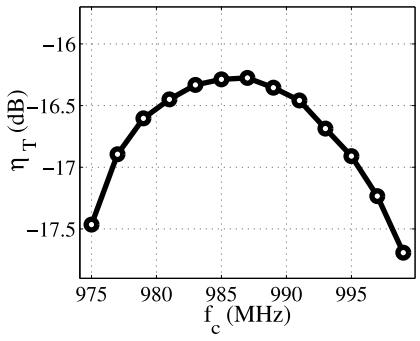
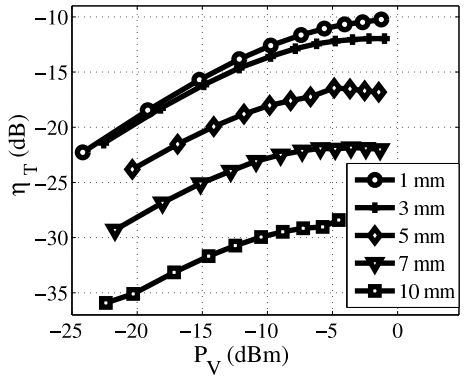
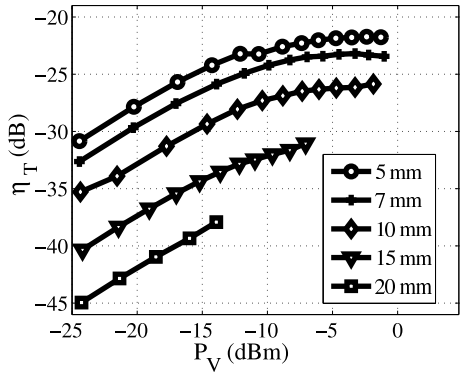


Fig. 20. The total efficiency was measured as a function of the carrier frequency when $d = 1$ mm, $d_{avg1} = 8$ mm and $P_{in} = 0$ dBm.



(a)



(b)

Fig. 21. Total efficiency measured for different distances with: (a) $d_{avg1} = 8$ mm. (b) $d_{avg1} = 22$ mm.

the range of P_V equals -5 dBm to 0 dBm, since the rectifier efficiency is higher within this range and also because the value of p is close to 1, which is its optimal value in the weak-coupling regime. The curves corresponding to the longer distances are incomplete, due to the limitation on the power level of the RF generator.

The efficiency is strongly dependent on the distance, especially for larger distances when the coupling is weak. At lower distances, this dependence decreases because of the proximity to the strong-coupling region (in this case, the input matching can degrade due to the coupling of the secondary). This explains why the 1 mm and 3 mm curves in Fig. 21(a) are very close to each other. To better visualize the dependence of the efficiency on the distance, the maximum points on each

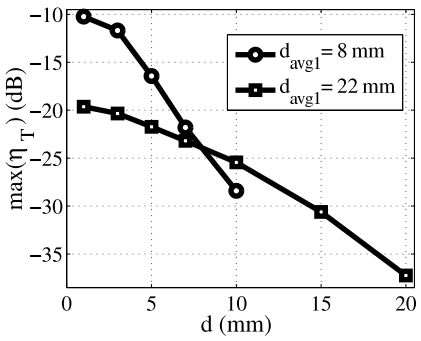


Fig. 22. Maximum total efficiency measured as a function of the distance.

TABLE III
INDUCTIVE LINKS WITH MONOLITHIC WPT RECEIVER.

	Area (mm^2)	Receiver technology	Q_2 (max.)	f (MHz)	η_{rlk} (%)	d (mm)	FoM
This work	2.3	CMOS 180 nm	21	986	7.26*	5	269
					0.93*	10	276
					0.29*	15	290
[15]	4.8	CMOS 130 nm	11	187	1.42**	10	159
[17]	20.3	High resistivity substrate and post-processing	20	7	4.3**	12	82
[13]	0.4	CMOS 180 nm	–	900	0.16	2	6
[11]	0.5	CMOS 130 nm post-processing	3	2450	0.02	0.5	0.01

$*$ Deducting $\eta_{com}\eta_{RT}$ simulated from η_T measured.
$**$ Maximum achievable gain from the two-port S-parameters.

curve of Fig. 21(a) and Fig. 21(b) are shown in Fig. 22. The inductor with a d_{avg1} value of 8 mm was designed for the nominal distance of 5 mm. For this reason, it presents better efficiency for distances less than 8 mm. On the other hand, the largest inductor presents better efficiency for distances greater than 8 mm.

E. Comparison with other studies

An interesting figure of merit (FoM) for inductive links containing miniaturized WPT receivers was proposed in [15]:

$$FoM = \frac{\eta_{rlk} \times d^3}{A_{Rx}^{3/2}}, \tag{27}$$

where A_{Rx} is the WPT receiver area expressed in mm^2, the d value is in mm and η_{rlk} is given as a percentage. The resonant link efficiency is used instead of η_{lk}; therefore, the quality of the impedance matching networks is also considered. In table III we compare some representative studies on inductive links with monolithic WPT receivers and it can be observed that our work achieves the best FoM. To separate η_{rlk} from the η_T measured values, it is necessary to know $\eta_{com}\eta_{RT}$. Even though we did not measure $\eta_{com}\eta_{RT}$ we have two estimations for it and both are plotted in Fig. 19(b). One curve was completely obtained from simulations and the other was obtained from the WPT efficiency measured under strong

coupling regime. We chose the simulated curve to calculate the η_{rlk} values reported in Table III because it represents the worst case for η_{rlk} between the two estimations. A high FoM was obtained because the design was focused on the optimization of each contributing factor in (10). Among these factors, it is important to emphasize the quality factor of the integrated inductor, which is greater than 20.8 (20.8 is the measured quality factor of the LC resonator). This performance is considered high for an inductor fabricated in a conventional CMOS process. The references [17] and [11] use post-processing steps to fabricate the receiver inductor, which could potentially improve its performance but with increased costs. Moreover, in [17] a high-resistivity substrate is used, thus minimizing the substrate losses. Regarding the measurement method, only the WPT receivers designed in [13] and that reported in this work were tested in a true contactless situation. Furthermore, the efficiency reported in [15] and [17] corresponds to the maximum achievable gain of the two-port S-parameters measurement. This method measures the inductive link efficiency but does not include the losses of the matching networks, which are mandatory in a complete system. It is important to note that the maximum quality factors in [15] and [17] occur at frequencies 101 MHz and 2.5 MHz respectively, which are lower than the reported frequencies at which the maximum link efficiencies occur. Thus, the quality factor at the point of maximum link efficiency is lower. In our work, the maximum quality factor of both transmitter and receiver inductors are obtained at the same frequency by using the segmented-inductor technique for the primary.

VI. Conclusions

A design method was proposed to optimize each factor that contributes to the efficiency of an inductive-link based WPT system. The optimality of the link efficiency is obtained by choosing the inductor dimensions and frequency that maximizes the primary and secondary inductor quality factors and the magnetic coupling factor. Also, the load is selected to optimize the p value. The theory was verified with simulations and measurements. The WPT receiver was constrained to be fully integrated in the $1.5\,\text{mm} \times 1.5\,\text{mm}$ area of a conventional CMOS 180 nm process. The main challenge in the WPT receiver design is to maximize the inductor quality factor, which was achieved through adequate selection of the inductor dimensions and a careful layout of the complete chip. The resulting inductor has one turn, an average diameter of 1210 μm and a linewidth of 250 μm. When resonating together with a Dual-MIM capacitor, the measured quality factor was 20.8 at 990 MHz, which is considered high for a CMOS integrated inductor. The transmitter inductor is fabricated on an FR4 board and its dimensions are selected so as to optimize the magnetic coupling and the quality factors. The use of a segmented inductor enabled the operation of the transmitter at the same frequency that optimizes the quality factor of the integrated inductor. For example, the optimal transmitter average diameter is 22 mm when the two inductors are separated by 15 mm. A strategy was developed to perform a true-contactless measurement of the WPT receiver. The efficiency measured in the case of the 15 mm distance is 0.29% and this performance leads to the best figure of merit reported to date, considering the size of the monolithic WPT receiver.

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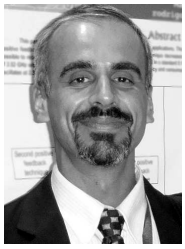
Fabian L. Cabrera was born in Colombia, in 1986. He received the degree in Electronic Engineering from the Industrial University of Santander, Colombia, in 2006, the M.Sc. degree in Electrical Engineering from the University of São Paulo, Brazil, in 2010, and the Ph.D. degree in Electrical Engineering from the Federal University of Santa Catarina, Brazil, in 2016.

From 2009 to 2012, he was with the Integrated Circuits Design House of the LSITEC, Brazil. He is currently a Professor at the Federal University of Itajubá - Itabira Campus, Brazil, where he is heading the research group Computation Applied to Engineering. His research has been mainly concerned with radiofrequency integrated circuits.



Fernando Rangel de Sousa (S'03-M'06-SM'13) received the B.Eng. and M.Sc. degrees in Electrical Engineering from the Federal University of Campina Grande, in 1996 and 2000, respectively, and the Ph.D. degree in Telecommunication and Electronic Engineering from Ecole Nationale Supérieure des Télécommunications (ENST), Paris, France, in 2004.

He is currently an Associate Professor with the EEL Department, Federal University of Santa Catarina (UFSC), heading a research laboratory focused on RF application s and wireless instrumentation. His research interests are primarily in RF Electronics, RFIC Design, Wireless Power Transfer and Wireless Instrumentation Electronics.