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A Duty-Cycle Controlled Variable-Gain Amplifier

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Abstract In this paper, a variable-gain amplifier (VGA) adjusted by the duty-cycle of a control signal is presented. This circuit is based on the superregenerative concept created by Armstrong back in the 1920's. The technique selected allows a fine control of the gain to be performed without any D/A converter at the interface between the digital control and the amplifier, as generally seen in other VGAs. An integrated-circuit version of the VGA was fabricated in a standard 180 nm CMOS process, aimed at achieving low-power consumption. Simulation results show a maximum gain of 45 dB within a 900 mV linear range, 0.5 % THD and a power consumption of 6.4 μW. Measurements on the chip were performed and the results corroborate the simulations.

Keywords Signal conditioning · Superregenerative amplifier · Variable gain amplifier · Analog design

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1 Introduction

Wireless body area networks (WBANs) have become an important research subject which will promote innovation in the near future [1, 2]. In a typical WBAN scenario, wireless sensor nodes are installed in or on the body of a person, requiring miniaturized solutions and, as a consequence, the use of small batteries or battery-free circuits. These ultra-low power systems are typically composed of one or more sensors, an analog front-end for signal conditioning, a processor unit and a transceiver.

As shown in Fig. 1, a biopotential analog front-end usually includes a variable-gain amplifier (VGA) which is commonly controlled by a digital circuit [3,4]. There is a common trade-off between gain resolution and area or complexity [5], which can affect the cost of the system. In this paper, we propose a VGA that can be controlled by the duty-cycle of a digital signal. This digital gain control makes this circuit a suitable alternative to common VGAs and PGAs due to its easy gain setting, since it eliminates the necessity for a D/A converter while preserving a high gain-step resolution [6]. The circuit is based on the superregenerative concept, which has regained the attention of the circuit designers in the RF field [7]. The superregenerative (SR) amplifier was idealized by Edward Armstrong, who aimed to develop a circuit capable of providing high gain with a low component count and, as a consequence, low power consumption [8]. In [9], the authors considered the application of the superregenerative technique in an amplifier for baseband signals, demonstrating the concept using discrete components.

In a previous study [6], the functionality of the baseband superregenerative amplifier was demonstrated as part of an automatic gain control (AGC) loop for

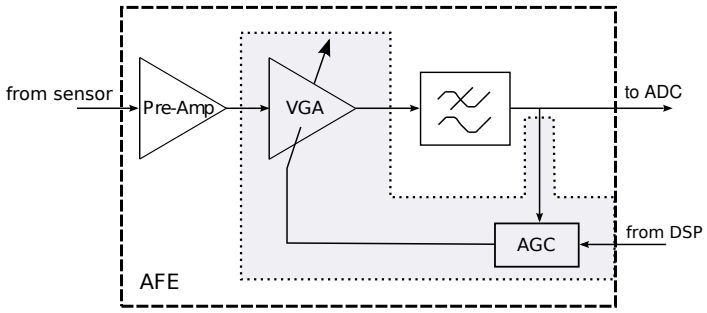


Fig. 1 General block diagram of an analog front-end (AFE) for biopotential signal acquisition.

biomedical signal acquisition. This implementation added two main features to the implementation in [9]: sampling the input signal in a differential configuration, to increase the rejection of the common-mode signal, and making the gain independent on the input source impedance by separating the sampling and the amplification phases.

In this paper, we extend the research described in [10] and [6] by reporting an integrated-circuit (IC) version of the amplifier implemented in [6], together with simulation and measurement results. The integrated circuit was designed in a 180 nm standard CMOS technology. Its core circuit is a negative resistance using a transconductor designed to compensate for low-frequency noise as well as offset voltage. Its power consumption was found to be 6.4 μW, with a gain range of 45 dB, this being suitable for low-power circuits such as WBANs or wireless sensor nodes.

2 SR amplification concept

In Fig. 2(a) we represent the concept of the VGA based on the baseband superregenerative amplifier. The circuit amplifies taking advantage of its periodically-reset unstable state. Its functioning principle is well-described in [6, 9].

In the time domain, the circuit responds as follows: first, the capacitor is discharged after closing the switch. The switch is then turned off and the input is connected to the amplifier. Since the circuit is unstable, the output will be an exponentially increasing voltage, which can be expressed by:

$$V_o(t) = w(t)V_{in}(t)\left(\frac{1}{R_G C_A} \times e^{-\frac{rem(t,T_{op})}{\tau_0}}\right) \tag{1}$$

where $V_{in}(t)$ is the input voltage source, R_G is the input-source impedance, T_s is the sampling period, T_{op} is the time for which the switch remains open at each sampling period, τ_0 is the time constant of the system given by

$$\tau_0 = (R_G // - R_l)C_A, \tag{2}$$

and $rem(x, y)$ is defined as the remainder after the division between x and y, and $w(t)$ is a window-type function defined as

$$w(t) = \begin{cases} 1 & \text{for } mT_s \leq t \leq mT_s + T_{op} \\ 0 & \text{for } mT_s + T_{op} < t < (m+1)T_s \end{cases}, \quad m = 1, 2, 3... \tag{3}$$

The circuit in Fig. 2(a) is designed for $R_l \ll R_G$ and thus the time constant in (2) approximates to $\tau_0 = -R_l C_A$, which is negative, thus explaining the exponential growth in (1). A typical output waveform of the amplifier is illustrated in Fig. 2(b). Each time the switch opens amplification takes place until it is stopped by closing the switch again; therefore, periodic exponential pulses can be observed ($V_o(t)$). The degree of amplification is dependent on the time for which the switch remains open and, as can be observed, the signal can achieve large values due to the exponential dependence on this period. By adding a sample-and-hold circuit working at the end of each pulse ($V_{SH}(t)$) and passing the sampled signal through

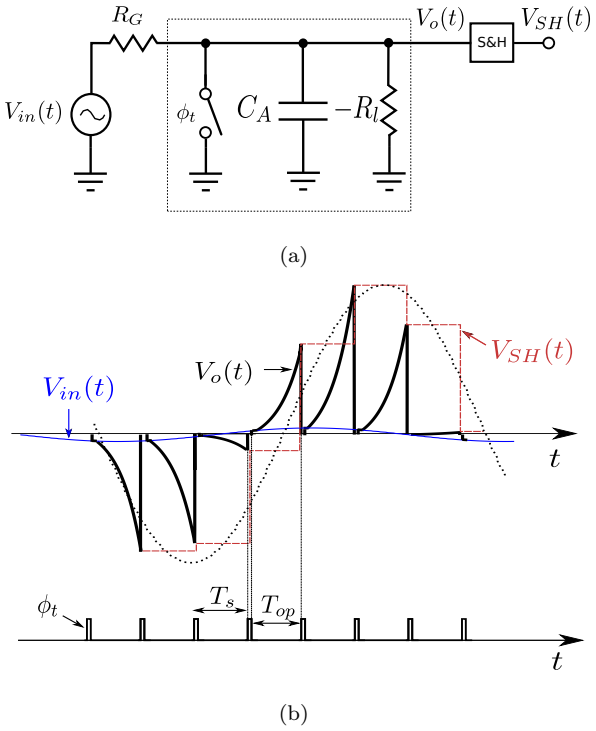


Fig. 2 Superregenerative amplifier (a) concept and (b) time-domain response.

a smoothing filter, a final amplified version of the input signal is obtained. It should be noted that a simple state machine, as implemented in our measurement setup detailed in the results section, can be used as the control signals generator.

3 SR baseband amplifier

The design of a superregenerative baseband amplifier is strongly dependent on the circuit which implements the negative resistance. The topology adopted in this study is shown in Fig. 3(a), where the negative resistance is obtained from an operational transconductance amplifier (OTA) configured in positive-feedback mode. This implementation is suitable for low-power consumption and does not require the use of resistors.

As explained in [6, 10], in relation to the circuit architecture, some switches are included in the circuit shown in Fig. 3(a) with the purpose of improving two main issues with respect to the implementation in [9]: first, the input signal is sampled in a differential configuration, which ideally eliminates the input common-mode signal. The second improvement is that the sampling and the amplification phases are performed separately, making the gain independent of the input source impedance.

The time response of the amplifier is expressed by (4)

$$V_o(t) = \sum_{m=1,2,\ldots} w(t) V_{in}(mT_{clk}) \left(e^{-\frac{t-mT_{clk}}{\tau}} \right) \tag{4}$$

where $V_{in}(mT_{clk})$ refers to the input signal sampled at the capacitor C_A at time mT_{clk}.

The VGA analyzed here in this paper has three operating phases, as shown in Fig. 3(b). The capacitor is discharged during each sampling period at phase ϕ_R. The signal source $V_{in}(t)$ is then connected to the amplifier capacitor C_A during the phase ϕ_S so that the signal is sampled with a sampling frequency $f_s = 1/T_{CLK}$. After the sampling phase, C_A is attached to the negative resistance. As a result, the sampled voltage in the capacitor is exponentially amplified until the control signal (ϕ_A) is disabled. As mentioned previously, the sample-and-hold circuit acts at the end of the amplification period (ϕ_{SH}) and further filtering is needed in order to reconstruct the output signal.

It can be easily proved that the OTA in positive feedback mode is equivalent to a negative resistor of value $\frac{-1}{G_m}$, where G_m is the OTA transconductance [11]. Hence, the VGA gain can be written as:

$$G(T_A) = e^{-\frac{T_A}{\tau}} \tag{5}$$

where τ is expressed as:

$$\tau = \tau_{OTA} = -\frac{C_A}{G_m} \tag{6}$$

As can be noted from (5), the gain is dependent on the duration of T_A.

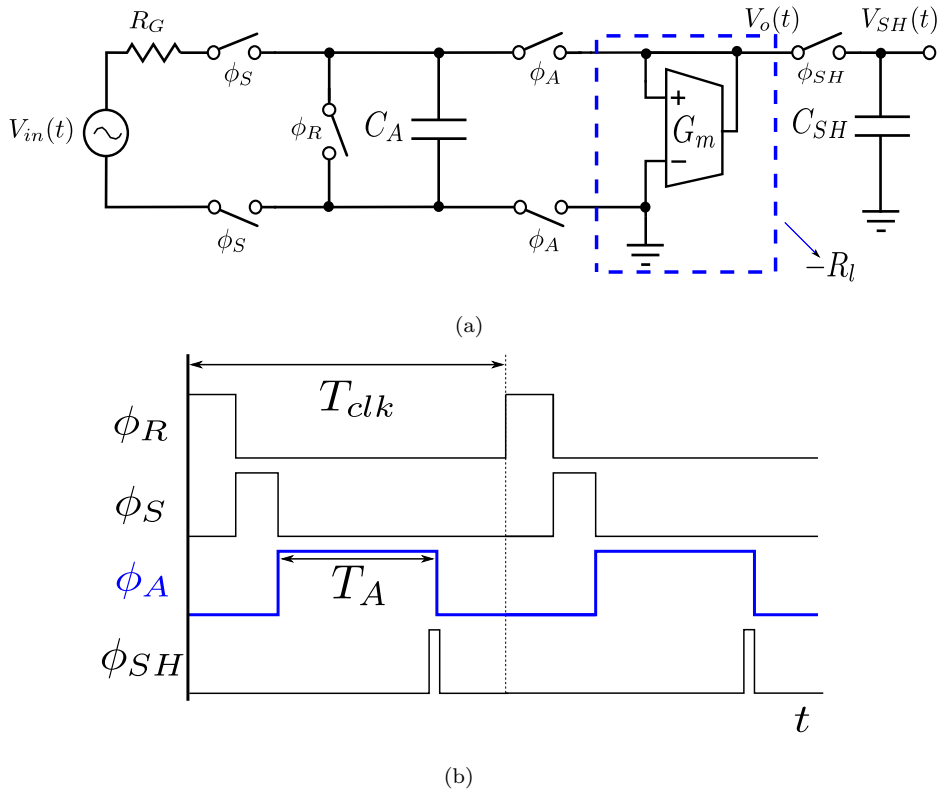
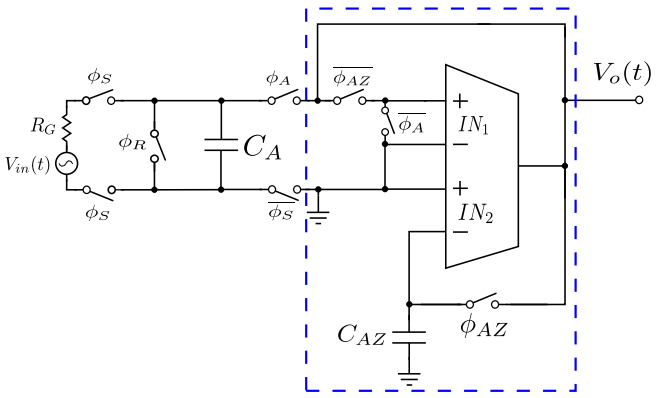


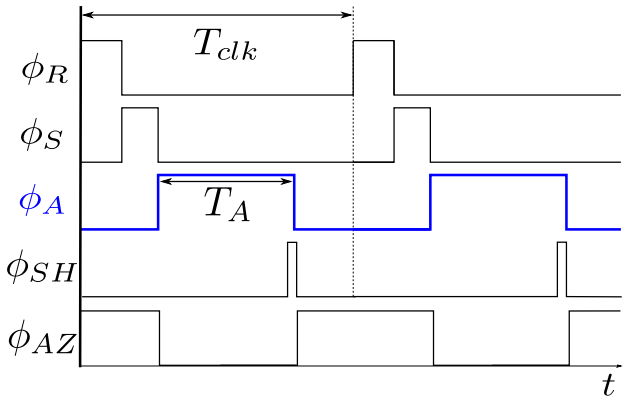
Fig. 3 SR - VGA (a) architecture under analysis and (b) corresponding timing diagram.

4 Integrated circuit implementation

We designed an integrated version of the SR amplifier, paying particular attention to the offset voltage compensation and linearity of the OTA, as described in the next section.



(a)



(b)

Fig. 4 OTA-based amplifier (a) schematic circuit including auto-zero technique and (b) corresponding timing diagram.

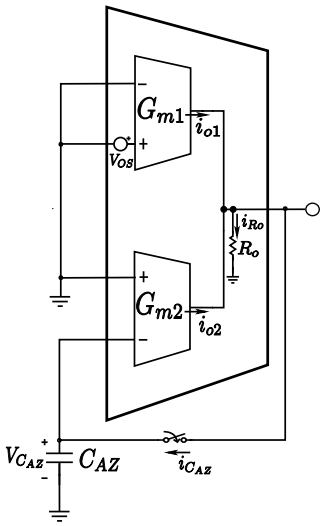


Fig. 5 Representation of OTA offset-compensation during the auto-zero phase.

4.1 Design considerations

The design of the VGA starts with the selection of the C_A capacitor value, which is important since it directly influences in the gain and the operating frequency of the circuit. Also, the total output noise of the circuit, assumed to originate mainly from thermal noise sources, is strongly dependent on the capacitor value, , as it is proportional to k_BT/C_A, where k_B is the Boltzmann constant and T is the temperature in Kelvin degrees.

Another issue to be considered in relation to the implementation of the proposed VGA is the non-idealities of the OTA. These include the input offset voltage, intrinsic noise, output impedance and linearity. Both offset voltage and low-frequency noise were addressed by adding the auto-zero technique. With the use of this technique we sought to reduce the variation in the gain during the amplification phase and prevent saturation of the circuit while working in a high-gain

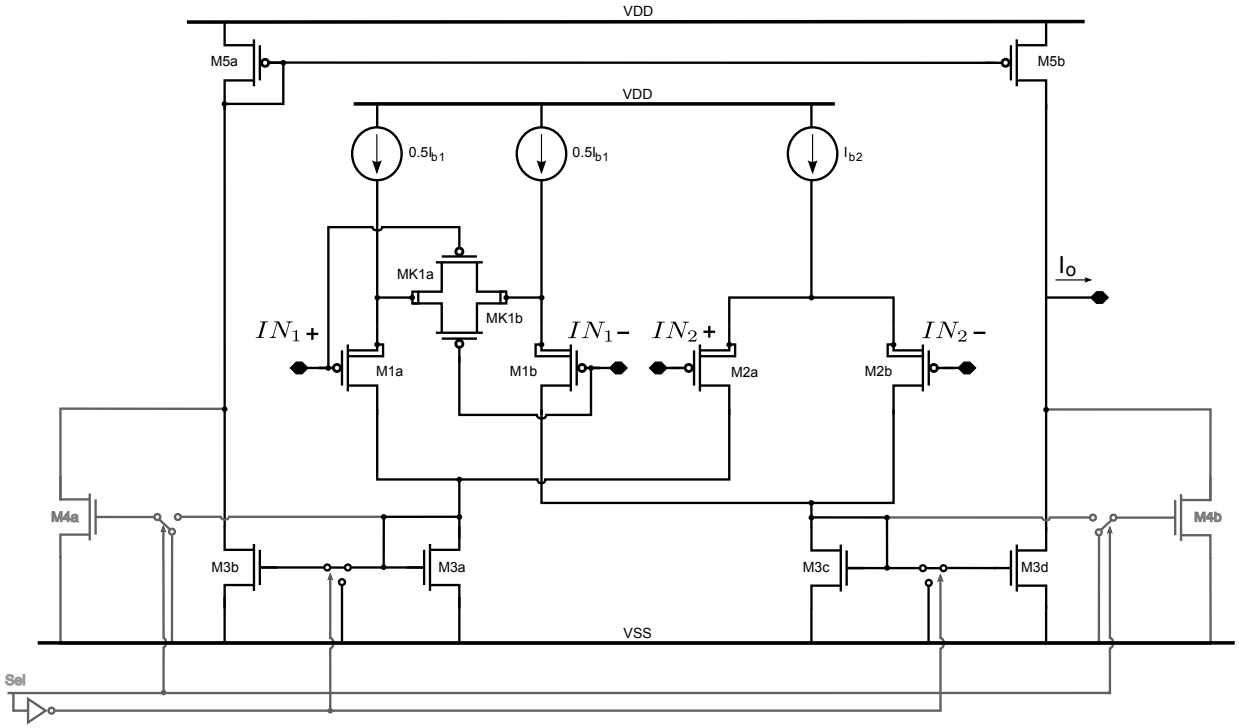


Fig. 6 Schematic diagram of the OTA used in positive feedback for negative resistance emulation, including double input for offset compensation. Cascode mirrors are not shown.

configuration, since the offset voltage of the low frequency noise could be even higher than a small input signal.

The final schematic diagram of the circuit with the addition of the auto-zero technique is shown in Fig. 4(a). As can be observed, a double-input OTA is required in order to produce the offset compensation. An extra control signal ϕ_{AZ} is also needed, as shown in the complete timing diagram in Fig. 4(b). Figure 5 aids an understanding of how the second input of the OTA compensates the offset in the main transconductor (G_{m1}) offset-compensation process. The offset compensation is performed while the circuit is out of the amplification phase: the OTA inputs (IN_1) are shorted ($\overline{\phi_A}$) and an output current proportional (i_{o1}) to its input

offset voltage is produced. When the switch controlled by ϕ_{AZ} closes, the compensation capacitor C_{AZ} starts to charge. If the output conductance of the OTA is high enough ($R_o >> 1/G_{m1}$) and we consider that the offset voltage at the second transconductor negligible, by choosing an appropriate transconductance ratio (G_{m1}/G_{m2}), then the voltage at the capacitor produces an output current from the second transconductor (i_{o2}) which will compensate for the first transconductor current until the current charging the compensating capacitor ($i_{C_{AZ}}$) reduces to zero. This voltage is then held during each amplification phase. Due to charge injection and finite output impedance, there will still be a residual offset [12], which should be estimated and considered during the amplifier design according to the system specifications. For our design, the maximum tolerated residual offset was considered to be 0.2 mV.

Besides the compliance with the auto-zero process, the OTA was designed to have sufficient linear ranges at the output and input, so that its transconductance is kept constant along the amplified signal swing, aiming at low distortion. A symmetrical single-ended topology with a degenerated input pair was selected. This topology also allowed the current consumption to be kept low. In order to increase the output impedance, cascode current mirrors were used.

A simplified schematic diagram of the OTA is shown in Fig. 6. An extra current mirror path activated by a selector was included. Thus, the transconductance could be switched between two values. A relation of 1 to 100 was selected with the aim of enabling flexibility in terms of the time constant. The final values of the OTA transconductance and the C_A capacitance were selected in order to achieve at least 40 dB within a bandwidth of 1 kHz. The transconductance ratio was set at 10, considering the dynamic range of the input signal and the residual offset tolerance.

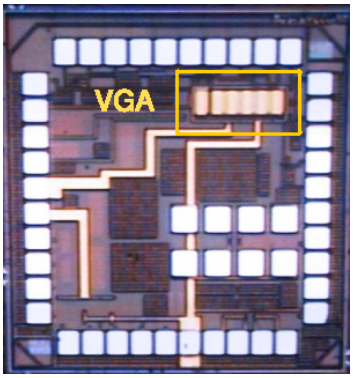


Fig. 7 Chip photograph.

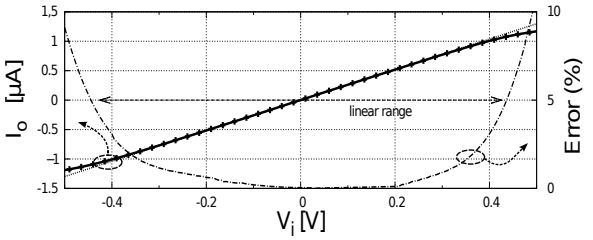
Appropriate layout techniques such as common centroid and interdigitation were used in order to reduce the offsets from the OTA. For C_A, a 100 pF dual-MiM capacitor was used, but an external pin was also included for the use of other external capacitors in parallel with the integrated one. In the photograph of the chip in Fig. 7 the top-metal capacitors layers can be observed. The capacitors were placed over the other analog blocks in order to reduce the effective circuit area.

4.2 Results

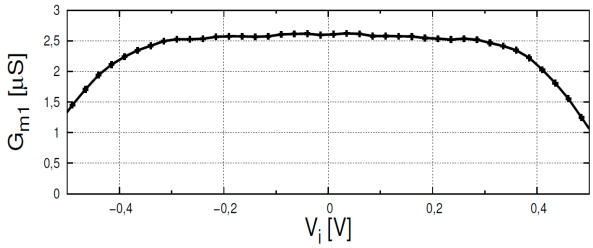
The circuit was designed in a 0.18 μm standard CMOS process with a 1.8 V supply voltage. The negative resistance was characterized by measuring the output current of the OTA while sweeping its differential input voltage with a 500 mV span centered at the common-mode voltage (analog reference). The results are reported in Fig. 8(a). The difference between the measured and the expected current of an ideal transconductor is also plotted. The linearity of the transfer curve was considered for a maximum current error of 5%. Therefore, the linear range was approximately 900 mV, that is, half of the supply voltage. Five chips were

measured and all presented the same linear response. From the measurement of the current, the transconductance was obtained considering its derivative with respect to the input voltage (Fig. 8(b)). The average value for G_m was 2.6 μS, which represents an equivalent negative resistance of 385 kΩ. This is in agreement with the results of the MC analysis which revealed a variation of 4% in 3σ in relation to the designed value of $G_m = 2.5\,\mu$S. The measured OTA consumption from the supply voltage was 2.7 μA, excluding the bias reference circuit.

The offset-compensation was evaluated by simulating the amplifier response through a purposely inserted offset voltage at the input of the OTA. This is shown in Fig. 9, where the transition between the moment before and after the insertion



(a)



(b)

Fig. 8 Measured (a) linear range of the OTA calculated from its output current as a function of the input differential voltage at IN_1, considering a maximum error of 5% from an ideal OTA response, and (b) transconductance obtained from its derivative with respect to the input voltage (V_i).

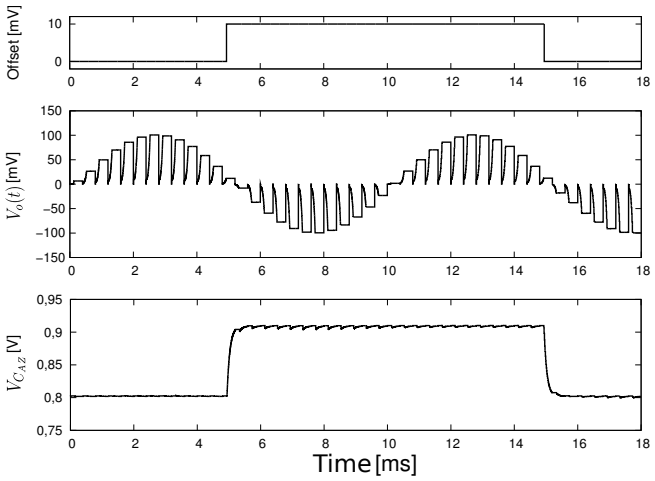


Fig. 9 Transient simulation results showing the amplifier output voltage response to a dynamically inserted offset-voltage in the OTA. The input signal is a 1 mV - 100 Hz sinewave and the amplification time was set at $T_A = 100\,\mu$s

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of the offset voltage does not cause a notable change in the output voltage. In contrast, the voltage in the compensation capacitor (shown below) senses and responds to the input offset voltage inserted, demonstrating that the auto-zero process implemented works correctly.

Deviations in the effective gain are expected from the variation in the G_m-transconductance and C_A-capacitance values. A 200-run MC analysis was performed from transient simulations of the VGA. A Verilog-A model of the transconductor was used, in order to accelerate the simulations. The simulation was designed to consider only the C_A-capacitance as the variable parameter and three values (nominal, bottom limit and top limit) extracted from the MC analysis of the G_m variation were fixed. The results are reported in Fig. 10. On average, the fluctuations in the capacitance values caused a standard deviation of 0.89 V/V. Considering 3σ, this was equivalent to 22% of the variation in the gain. On the

other hand, the (3σ) gain variation due to transconductance alone was smaller, representing almost 11% of the typical gain.

Measurements of the VGA were performed generating the control signals with a finite-state machine implemented in a FPGA development board. On measuring the VGA with the integrated C_A capacitor there was a DC component coupled with the input AC signal, which suggested that the charge-injection effect was greater than that expected. This effect decreased when using the output capacitor configuration ($C_A = 10\,\text{nF}$ and $G_m = 250\,\mu\text{S}$). An output-voltage signal as a response of an sinusoidal input signal is shown in Fig. 11. The output signal was also passed through a sample-and-hold circuit. The measured gain was around 10.5 V/V.

Finally, a characteristic curve for the gain-versus-duty-cycle was extracted from simulations and measurements, which can be seen in Fig. 12. The gain shows an exponential dependence on the amplification time, as predicted by (5). For high gain measurements, the OTA exceeds its linear range. The estimated maximum gain was of 45 dB, keeping the total harmonic distortion at less than 0.5%.

The main figure of merits of the VGA are summarized and compared with other state-of-the-art solutions in Table 1. A higher gain range was achieved compared to

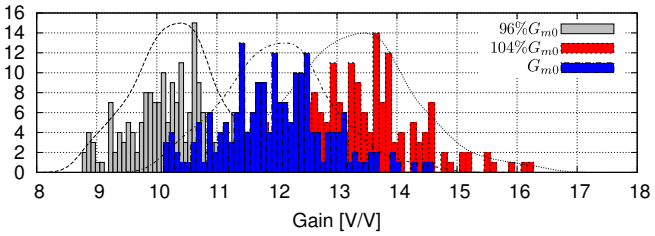

Fig. 10 MC transient-simulation results for $T_A = 100\,\mu\text{s}$ considering variations in C_A and G_m, where G_{m0} is the simulated value for the average transconductance.

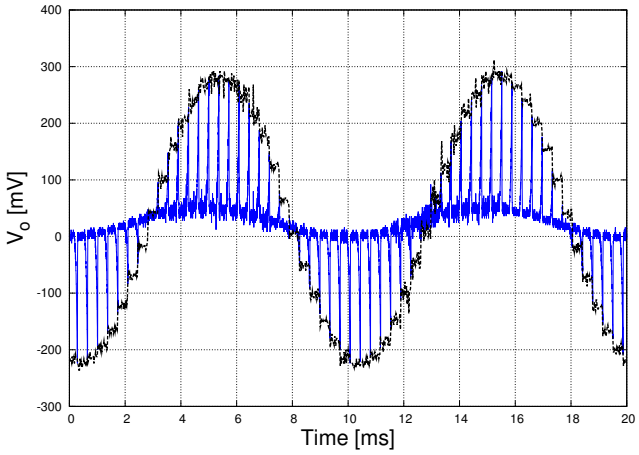

Fig. 11 Measured output of the circuit and its sample-and-hold version obtained from a 100 Hz-25 $\mathrm{mV_p}$ input signal, at $C_A = 10\,\mathrm{nF}$, $F_{clk} = 5.5\,\mathrm{kHz}$ and $T_A = 100\,\mu\mathrm{s}$.

the studies reported in [13] and [14]. In the case of the research described in [15], the circuit was intended to be used as the first front-end block and thus much higher power consumption was invested to obtained both a higher gain range and lower noise. In the case of [13], the area was smaller and the power consumption was lower compared with our work. However, we consider that the main contribution of this study to be the continuous gain control, which corresponds to the duty-cycle digital signal control.

Table 1 Comparison of results

Parameter	[13]	[14]	[15]	This work
Gain range [dB]	6 – 20.8	16 - 28	10 – 62	16 – 45
Gain steps	4	16	Continuous	Continuous
Consumption [μW]	0.5	2	280	6.4
Area [$\mathrm{mm^2}$]	0.05	0.25	0.064	0.08
Supply voltage [V]	1	1.7	$\pm$1.5	1.8
Process	0.35 μm	0.18 μm	0.35 μm	0.18 μm

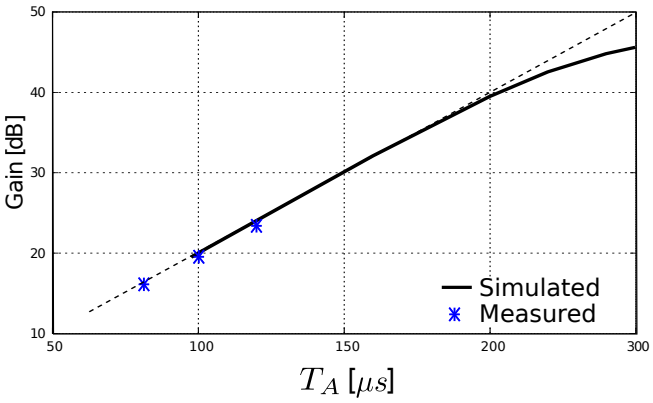

Fig. 12 Simulated and measured gain vs amplification time plotted which shows the exponential dependence of the gain on the duty-cycle of the control signal.

5 Conclusions

In this paper, we have described a superregenerative variable-gain amplifier suitable for biomedical signal acquisition. The amplification technique was based on the superregenerative concept created by Edward Armstrong. Architectural improvements in relation to a previous discrete-component implementation were proposed. A negative resistance based on a programmable-transconductance OTA suitable for the auto-zero technique was implemented in a standard 180 nm CMOS technology. The simulated results provided a maximum gain of 45 dB within a 900 mV linear range and a 0.5 % THD, while consuming 6.4 μW. Measurements verified that the circuit works properly, and the measured gain was in accordance with the variation expected based on the component tolerances, which was predicted using Monte Carlo simulations. The amplifier was found to be suitable for low-power analog front-ends in a closed-loop configuration which require fine gain control.

Acknowledgements The authors would like to thank CNPq for financial support and the MOSIS program for the test chip fabrication. Also, we thank Gabriel Manoel Da Silva for helping with the VGA measurements.

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