Variable Gain CMOS LNA

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ABSTRACT

In this paper it is presented a variable gain low noise amplifier (LNA) with differential output using a 0.18 μm CMOS technology. The design of this LNA was specified for a sigma-delta digital receiver, in accordance to the IEEE802.15.4 standard using the industrial, scientific and medical (ISM) band.

1. INTRODUCTION

The Low Noise Amplifier (LNA) is an essential block of a RF system. Its function is to provide gain, add a small quantity of noise while it deforms the signal as minimal as possible. Fig. (1) shows a simplified schematic of the receiver system that is being studied. This paper focuses on the LNA design for a ZigBee (IEEE802.15.4 standard) front end receiver.

Table 1 shows the specifications taken for the LNA design. These specifications were achieved by taking into account the ZigBee protocol and the sigma-delta converter.

For the design, it is also necessary to know the behaviour of the input impedance of the sigma-delta converter. A simulation of this impedance shows a tuned behaviour with a real value as high as 2 kΩ, in the band of interest, while the imaginary part has a low value.

Table 1: LNA's Specifications

Specification	High Gain	Low Gain
Voltage Gain	20 dB	0 dB
Noise Figure	< 3.5 dB	< 8 dB
Return Loss	< -10 dB	
Switch Mode	-65 dBm	
IIP3	> -13 dBm	
BW	80 MHz @ 2.442 GHz	
Max Input Power	-20 dBm	
Output Type	Differential	
Technology	Standard 0.18 μm CMOS	

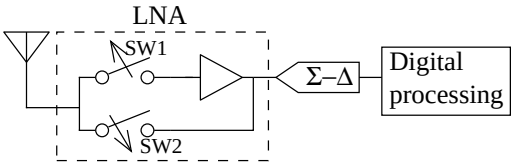

Figure 1: Receiver System

2. LNA CIRCUIT DEVELOPMENT

In this section it is presented how the thermal noise behaves in a common gate configuration, the topology chosen for the variable gain LNA, the simulation results, and the circuit's layout.

2.1 Noise Using the Common Gate Configuration

Since the noise requirements are not restrictive as shown in Table 1, the design of a common gate LNA (CG-LNA) is considered. It is already proved that the minimum noise performance for the CG topology is worse than a common source (CS) one [7]. However, it is interesting to understand how the noise figure (NF) behaves in the CG topology for the MOS transistor. To do this, Fig. (2) shows the small signal model for intermediate frequencies of a two port intrinsic transistor using the CG configuration. Where g_{ms} is the source transconductance and vs the source voltage. In Fig. 2 (a), the transistor is seen as a noisy element with the channel thermal noise represented as i_{nch}. And in Fig. 2 (b), the transistor is seen as a noiseless element with the thermal noise referred to its input shown by the en and the in sources.

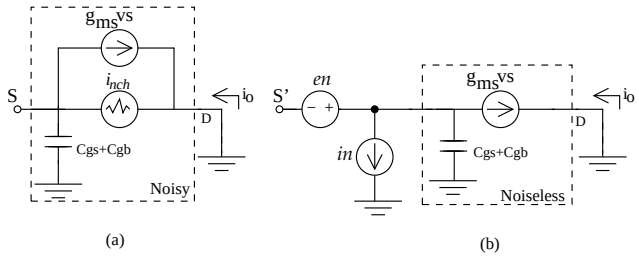

Figure 2: Two port small signal representation. (a) Transistor as a noisy element, (b) transistor as a noiseless element

The first step to calculate the noise factor is to find the rela-

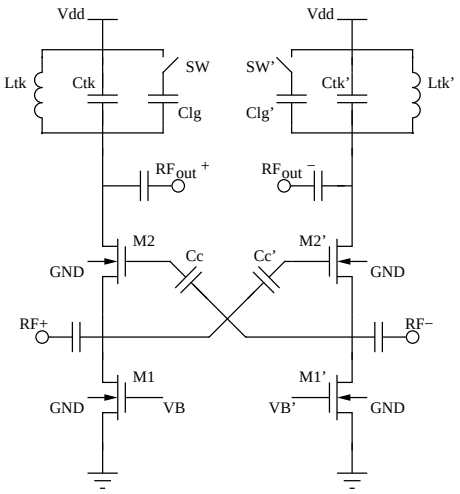

Figure 3: LNA's schematic

tionship between the noise sources en and in with respect to the channel thermal noise i_{nch}. In the next step to find the noise factor, a signal source with a series resistance equal to Rs is inserted in terminal S' [5]. By doing this, the noise factor is found as:

$$F - 1 = \frac{\gamma}{g_{ms}} \left(Rs^2(\omega C)^2 + \frac{1}{Rs} \right) \tag{1}$$

where γ is the excess noise of the MOS transistor and C is the total source capacitance. Using $1/g_{ms} = Rs$, $\gamma = 2/3$, and neglecting the term with the capacitance, one can find that the noise figure is [7]:

$$NF \cong 10 \log(1 + \gamma) \cong 2.2\,\text{dB} \tag{2}$$

2.2 LNA's Topology

The LNA schematic can be seen in Fig. 3 where, for simplicity, the biasing circuits are not shown. This schematic shows an interesting technique using capacitors Cc and Cc' called cross coupled capacitors presented by [9]. A signal with opposite polarity of the source of M2 transistor is applied to its gate. This voltage signal is determined by the capacitive voltage division (A) which can be calculated as [10]:

$$A = \frac{\text{Cc}}{\text{Cc} + C} \tag{3}$$

Considering the transistor M1 and M1' as an AC open circuit, instead of being similar to $1/g_{ms}$ the transistor input impedance seen from the RF+ or RF- node becomes:

$$Z_{in} \cong \frac{1}{g_{ms} + A g_{mg}} \cong \frac{1}{g_{ms}(1 + A/n)} \tag{4}$$

where g_{mg} is the gate transconductance and n is the MOS transistor slope factor [6].

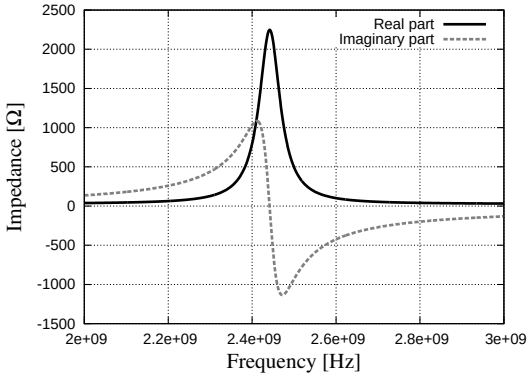

Figure 4: Simulated input impedance of the Sigma-Delta converter

Similarly, the noise factor becomes:

$$F - 1 \cong \frac{\gamma}{(1 + A/n)} \tag{5}$$

Hence, this topology can decrease the noise figure of the CG-LNA as shown in [9, 10]. Due to area restrictions, the inductors in the source of M2 and M2' found in [9, 10], are replaced by M1 and M1' MOS transistors for DC biasing. The tank inductor (Ltk, Ltk') and the tank capacitor (Ctk, Ctk') are made to resonate in the desired band.

However, the capacitors Clg and Clg' are designed to change the resonance to a lower frequency when the switches SW and SW' closes. Also the drain current of the transistors can be decreased to decrease the transistor transconductance and hence, the gain. Therefore, the small gain mode is achieved by switching on SW and SW' and by reducing the current consumption.

2.3 Results

The LNA's load (input stage of the sigma-delta converter) has a differential input and the simulated value of its impedance in each input can be seen in Fig. 4.

To make the simulations of the LNA's performance, its input has an ideal balun which is used to generate the signals RF+ and RF-. And for its output, the sigma-delta input impedance value is used. Fig. 5 shows the voltage gain behaviour of the amplifier that has a 3 dB bandwidth of 177 MHz in the high gain mode. In the low gain mode, the tank resonance shifts and the gain decreases at 2.4 GHz. Fig. 6 and Fig. 7 show, respectively, the LNA's characteristics of the noise figure and of the return loss.

The final layout is shown in Fig. 8 where the inductor, which has an equivalent inductance of 4 nH at 2.4 GHz, has a dimension of $400\,\mu\text{m} \times 400\,\mu\text{m}$. And the total area of the LNA with the pads is $1500\,\mu\text{m} \times 850\,\mu\text{m}$ ($1.27\,\text{mm}^2$) .To help with the measurements, an active balun [2] and two buffers with output impedance of $50\,\Omega$ are implemented in the input and output of the LNA respectively. Also, it is important to note that pads, metal lines inside the circuit or connecting it to he pads, introduce parasitics, which are responsible for a degradation of the system performance. Hence, for

Table 2: Comparisons between differential CMOS LNAs

Parameter	[1]	[2]	[3]	[4]	This Work
Frequency (GHz)	2.45	0.2-5.2	2.2	2.0-3.5	2.44
Gain (dB)	16.8*	13*-15.6*	8.6	26.2/12.5 @2.4 GHz	21*/-0.1*
Noise Figure (dB)	1.24	< 3.5	1.82	2.9/7.4	2.8/6.3
Return Loss (dB)	-21.2	-15	<-13	<-10 / >-10	-17/-13
IIP3 (dBm)	12.6	> 0	-2.5	-8/0	-3/-9
Core Current Consumption (mA)	-	-	2x4.5	10.6/11	2x1.5/2x0.75
Total power consumption (core) (mW)	(4)	21 (14)	(16.2)	19.08	11.1 (5.4)/6.9 (2.7)
Dimensions (μm $\times$ μm)	NA	110×80	1300×1000	1600×730	1500×850
CMOS Technology	0.18 μm	65 nm	0.35 μm	0.18 μm	0.18 μm
Supply Voltage (V)	1.8	1.8	1.2	1.8	1.8

the de-embedding, three structures using short, open, and through for the LNA, for the active balun, and for the buffer were built. One example of these structures can be found in [8]. Table 2 shows a comparison with other recent works. Where, the slash mark (/) separates the performance values between the high and the low gain modes, and the asterisk mark (*) stands for for the voltage gain values.

3. CONCLUSIONS

The simulations results show that it is possible to have two modes of gain and meet the required specifications. Since the core consumption is reduced, an elegant way of making the low gain mode is achieved. Therefore, this LNA is being fabricated using a 0.18 μm CMOS technology.

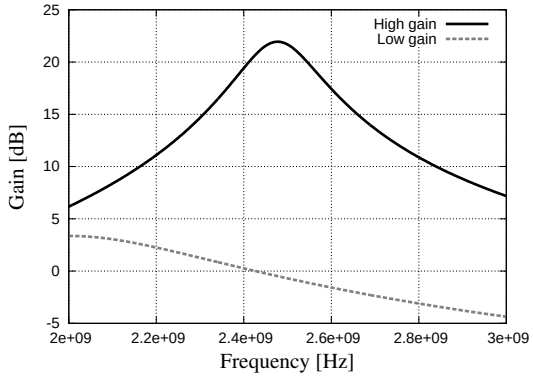

Figure 5: Simulated voltage gain of the LNA

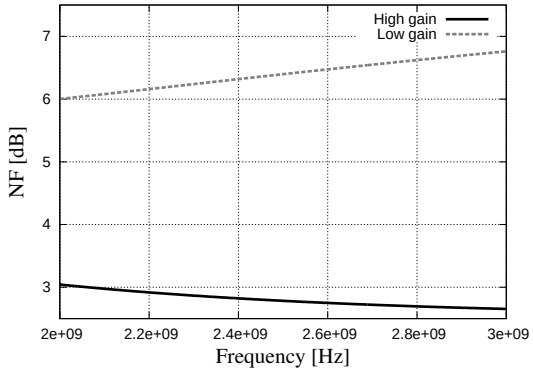

Figure 6: Simulated noise figure of the LNA

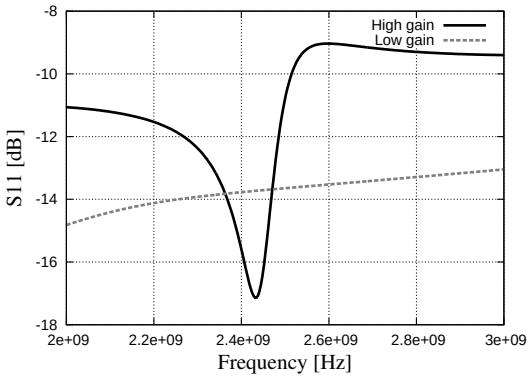

Figure 7: Simulated return loss of the LNA

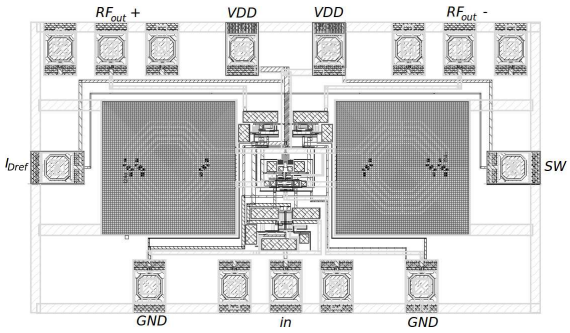

Figure 8: Layout of the LNA

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