Duty-cycle Controlled Variable Gain Amplifier

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ABSTRACT

A variable gain amplifier (VGA) is proposed as part of a sensor interface for portable biomedical applications in which ultra-low-power analog processing is required. The particular characteristic of this VGA is that its gain can be controlled by a clock signal duty-cycle. Auto-zero technique is also employed for reducing the low-frequency noise and offset. The circuit was designed in standard 0.18 μm CMOS process and has been sent for fabrication. Post-layout simulation results predicts the expected response of the VGA.

1. INTRODUCTION

Intercommunication among sensor nodes in or around the human body, which is currently named as Wireless body-area networks (WBAN), is a hot spot in electronics development for healthcare. These portable medical systems are meant to work for long periods of time in order to achieve certain level of autonomy. This fact is the one that determines the power consumption of the electronic circuits. Therefore, strong efforts are made at system and circuit level for building ultra-low-power analog front-ends and transceivers. The power budget assigned to each of the blocks inside these units and the correct distribution of functionality between analog and digital parts are critical for obtaining low power consuming chips [1].

This work falls within the scope of designing a biopotential read-out ASIC, suitable for a wide range of biomedical applications. This read-out circuit needs to achieve several requirements such as power consumption, input impedance, bandwidth and noise. Adding adjustable gain and bandwidth to a read-out circuit is necessary since its characteristics can be adapted depending on the biopotential signal of interest [2], [3]. In this context, this document presents the design of a novel architecture of a variable gain amplifier (VGA) intended for low-frequency signals in low-power medical applications. This circuit is intended work as a gain stage for delivering an optimum voltage swing signal to another circuit, which could be an analog-to-digital converter.

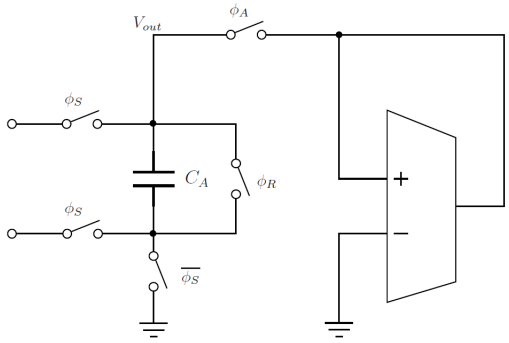

Figure 1: Schematic circuit of the VGA.

The objective of this work is to develop an analog IP that can be used as a flexible analog block in integrated circuits for biomedical purposes.

2. THE PROPOSED ARCHITECTURE

The concept of the VGA is depicted in Fig. 1. The circuit is essentially composed of a capacitor (C_A) and an operational transconductance amplifier (OTA). The VGA have three main operation phases represented in Fig. 2. The timing diagram is shown in Fig. 3 (ϕ_{AZ} not considered for now). First, in the reset phase (ϕ_R), both terminals of C_A are shorted to analog ground. Then, the sampling period (ϕ_S) is enabled, so the capacitor is charged to the input signal (V_{in}). After some appropriated time for signal settling, the amplification period (ϕ_A) is enabled. In this phase the capacitor is connected to the OTA. Notice that the OTA is in a positive-feedback configuration. The objective of this is to emulate a negative resistor equal to $\frac{-1}{G_m}$, where G_m is the OTA transconductance. As a consequence, the sampled voltage in the capacitor will be amplified exponentially [4].

The amplified voltage for each clock period (T_{clk}) can be expressed as in (1). It is clear that the final gain depends on the ratio between the duration of the amplification signal pulse (T_A) and the time constant of the circuit (τ), which is expressed in (2). Therefore, the gain of the VGA can be controlled by ϕ_A duty-cycle, which is defined with respect to the complete clock period. The output voltage of the VGA (V_{out}) will have the shape of a series of exponential pulses. In order to obtain the final amplified signal, a sample-and-hold circuit must be added.

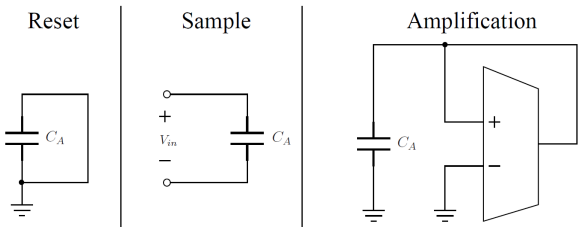

Figure 2: Operating phases of the VGA.

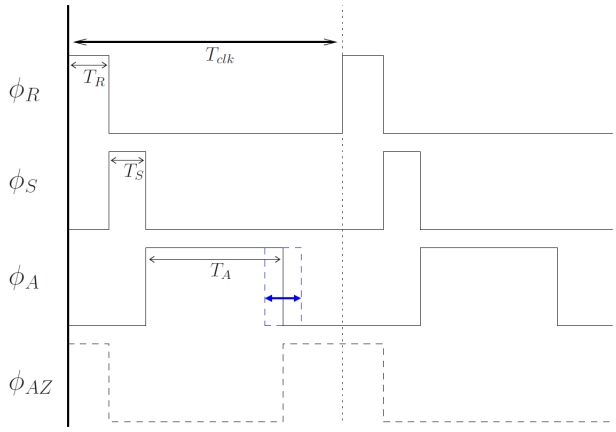

Figure 3: Timing diagram of the VGA.

$$V_{out} = V_{in}\left(e^{-\frac{T_A}{\tau}}\right) \tag{1}$$

$$\tau = \frac{C_A}{-G_m} \tag{2}$$

The circuit of the VGA presented suffers from an important drawback: The input offset voltage together with the low-frequency noise of the OTA can be significantly bigger than the input signal, which implies that the input signal will be buried under non-useful information. Moreover, these non-idealities can cause saturation of the output voltage for high enough gain configuration of the VGA. For these reasons the complete circuit includes the autozero (AZ) technique for reduction of the impact of these issues. The final schematic of the VGA is shown in Fig. 4. The OTA presents two inputs since the open-loop offset cancellation principle is implemented [5]. The normal amplification process is performed by IN_1, while the second input IN_2 is used for autozeroing. A new clock signal (ϕ_{AZ}) is required for the control of the AZ process, as shown in dashed lines in Fig. 3. While this signal is enabled, the capacitor C_{AZ} samples a voltage proportional to the first-input referred offset of the OTA and then holds it during the amplification period.

3. THE DESIGN OF THE VGA

Since the proposed VGA has a sampled nature, Nyquist criteria has to be taken into account. In this work, the operating frequency of the VGA (f_{clk}) is set to be at least ten

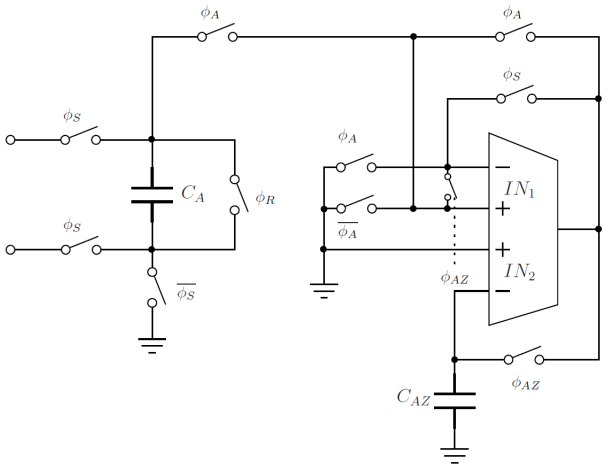

Figure 4: Complete schematic circuit of the VGA.

times the bandwidth of the input signal. This fact delimits the values for C_A and G_m, as seen in (2). Ideally, the contribution on the total circuit noise would come from the thermal noise sampled by C_A, since the flicker noise of the OTA is cancelled by the AZ technique. Thus, depending on the minimum amplitude of the input signal, the capacitor value can be determined. Then, a suitable value for G_m is chosen in order to be able to work at the correct operating frequency. G_m is also limited by the power consumption budget, so usually low transconductance in the order of μS might be chosen.

The topology chosen for the OTA was the symmetrical one shown in Fig. 5. Both input pairs of the OTA are pMOS type, and the transconductance associated to IN_1 was designed to be ten times higher than the associated to IN_2. This consideration relaxes the thermal noise contribution of the autozero capacitor. An important aspect on the OTA design is the linearity. When the voltage of the capacitor increases, the differential input voltage of the OTA also does.

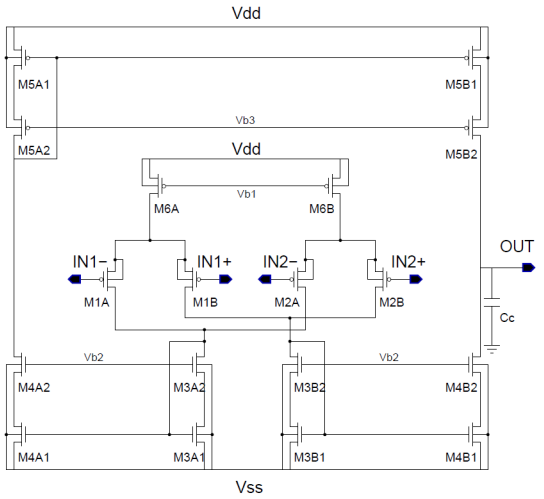

Figure 5: Two-input OTA.

To maintain the response equal to (1), the OTA transconductance should remain constant. The inversion level of the main input pair was chosen in order to achieve ±120 mV input-voltage range of linear response with a 5% of error. Its gate-area was chosen large enough for maintaining the 3-sigma input-offset voltage less than 3 mV. The low frequency open-loop voltage gain of the OTA was designed to 80 dB and 60 dB, respectively for each of the inputs.

Some extra switches (not shown in Fig. 4) were added for test purpose. For testing the reliability of the VGA against noise, both the amplification and the auto-zero capacitor connections includes external pins to add more capacitance to the already integrated capacitors of 10 pF each. The switches were designed using complementary MOSFETs with dummy structures for reducing the charge injection and clock feed-through effects.

4. RESULTS

The design of the VGA was realized in XFAB 0.18 μm with a supply voltage of 1.8 V. A DC sweep was done for verifying the OTA linearity and the results are shown in Fig. 6. The OTA achieves a linear range of ±120 mV with 5% of error. The mean value of the transconductance referred to the first input of the OTA was estimated by a 100-run Monte Carlo simulation with process and mismatch variations. The results are shown in Fig. 7. The variation on the linearity error was also estimated, as shown in Fig. 8. Considering all these results, the estimated variation on the time constant τ due to process and mismatch variations will be less than 5%. Since the VGA is expected to work inside an Automatic Gain Control (AGC) loop in which the gain will be automatically adjusted, this variation is easily compensated. The OTA consumes almost 115 μA including its bias circuit.

For the transient simulation of the VGA, a duty-cycle of 35% was selected for an operating frequency of 30 kHz. The plot of the output voltage is shown in Fig. 9 where an input signal of 1 mV and 1 kHz was applied to the VGA. The plot shows the pulsed nature of the response and an approximated gain of 100. The dashed line shows an ideal reconstruction after a sample-and-hold circuit and a filter. In addition, post-layout simulation results of the variable gain as a function of the duty-cycle of ϕ_A are shown in Fig. 10. The gain follows a constant exponential dependence until the value in which the OTA is out of its linear region. These results corroborate the simulated linear range of the OTA shown previously. The layout of the submitted circuit is shown in Fig. 11.

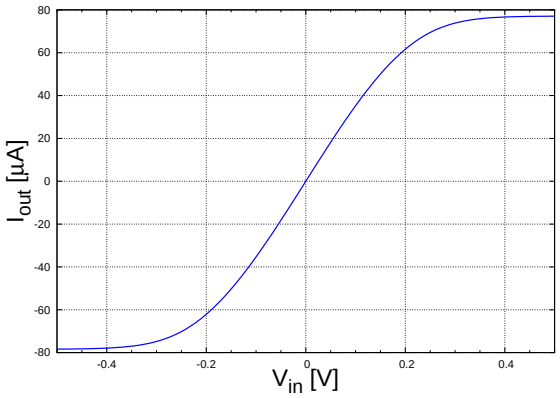

Figure 6: Variation on the OTA output current due to the input differential voltage applied in IN_1.

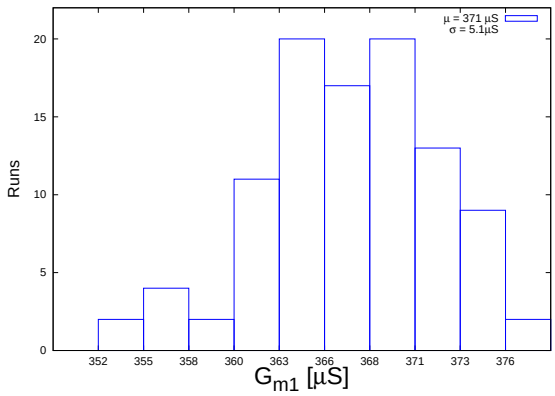

Figure 7: Simulated variation of the OTA transconductance referred to the first input due to process and mismatch.

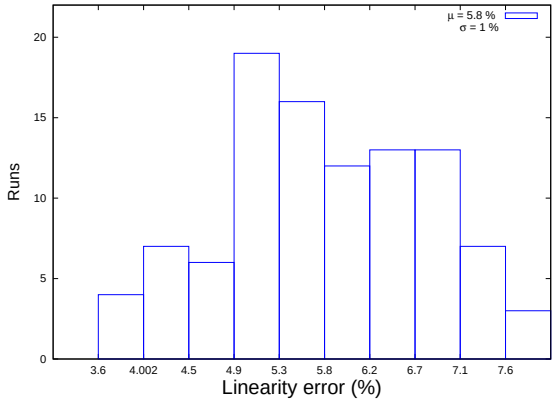

Figure 8: Simulated variation of the OTA linearity error @ $V_{in} = \pm 120$ mV due to process and mismatch.

5. CONCLUSIONS AND FUTURE WORK

A novel architecture of a variable gain amplifier was presented. This circuit will be part of an analog front-end read-out circuit for bio-potential signals. Post-layout simulations corroborates the expected results from the proposed circuit.

This prototype was not optimized for power consumption since the first objective was to validate the work-principle of the circuit. Improvements in the OTA design must be done for achieving higher linearity without compromising area, power and noise. Noise evaluation of the circuit is determining for considering a total integrated solution, due to the sampling/amplification capacitors. Finally, this VGA has to be evaluated inside a read-out circuit for biomedical signals where an AGC is implemented.

6. REFERENCES

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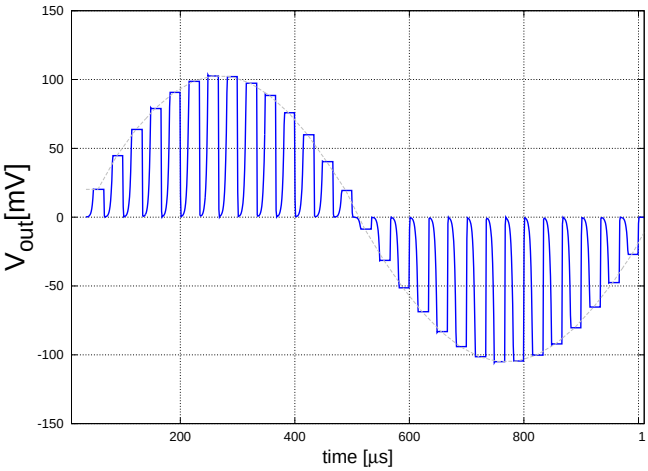

Figure 9: Response of the VGA for a duty-cycle of 35% for a 1 mV 1 kHz input signal.

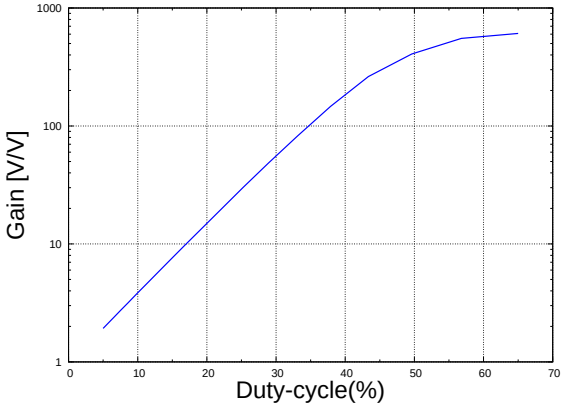

Figure 10: Gain as a function of the duty-cycle.

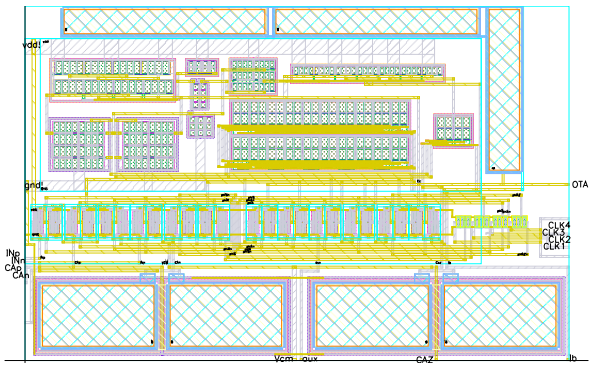

Figure 11: Layout of the VGA.