A Duty-Cycle Controlled Variable-Gain Instrumentation Amplifier Applied For Two-electrode ECG Measurement

R. Romero Antayhua, G. Manoel Da Silva, F. Rangel de Sousa
Integrated Circuits Laboratory-LCI
Federal University of Santa Catarina-UFSC
Florianopolis-SC, Brazil, Tel.: +55-48-3721-7640
Email: {roddy.romero; gabriel.manoel; rangel}@ieee.org

***Abstract*—An instrumentation amplifier with variable gain suitable for biopotential signal acquisition is presented. The architecture proposed is based on the superregenerative receiver created by Armstrong back in the 1920's. It allows controlling the gain by the duty-cycle of a digital clock. This feature reduces the complexity for implementing an automatic gain control circuit, since no digital-to-analog converter is needed in the interface of the gain control. The implemented instrumentation amplifier provides a variable gain of $40.2\,\mathrm{dB}$ with a $0.5\,\mathrm{dB}$ gain-step resolution, plus a fixed gain of $28.2\,\mathrm{dB}$, giving a total gain range of $68.2\,\mathrm{dB}$ dB. It was evaluated by acquiring ECG signals using only two electrodes installed on the body of a volunteer. Results show that the amplifier acquires the ECG signal and that it is capable of adapting its gain to a specified voltage amplitude for delivering it to an A/D converter.**

I. Introduction

The Analog Front-End (AFE) of a medical acquisition system is in charge of conditioning the signals coming from sensors installed on the human-body, which are often weak and their spectrum covers from DC until some tens of kHz [1]. Commonly, an AFE includes stages of amplification, filtering, and an Analog-to-Digital Converter (ADC), which makes the interface with the Digital Signal Processor (DSP) [2], [3]. The amplification performed by the AFE is chosen according to the expected nature of the signal, i.e. for different signals such as EEG, ECG, EMG, among others, a specific gain range is used. Moreover, if the AFE includes a low/medium resolution ADC, it is preferable that the gain is adjusted to the full scale of the ADC dynamic range. This can be implemented by means of an Automatic Gain Control (AGC). Hence, a Variable Gain Amplifier (VGA) as part of the AFE is required [4].

Most analog front-ends for biomedical applications use digitally controlled Programmable Gain Amplifiers (PGA) for setting its gain, since they simplify the gain control interface by removing the digital-to-analog converter usually needed for VGAs [5]–[7]. However, the low fixed number of bits used for gain programming limits the gain-step resolution, reducing the performance of the AGC. Due to the fact that many medical acquisition systems include a microcontroller for signal processing [8], a digitally-controlled VGA turns to be an ideal solution.

In this paper, we propose an Instrumentation Amplifier (IA) suitable for biopotential measurement with variable gain, controlled by the duty-cycle of a digital clock signal. The IA uses a non-conventional amplification technique based on the superregenerative receiver principle introduced by Armstrong [9] and more recently explored for baseband signals in [10]. The IA is composed of two stages. The input stage controls the common-mode input signal usually present due to the $50/60\,\mathrm{Hz}$ interference power line. The second stage is the variable gain amplifier which is based on the amplifier reported in [10]. Their implementation suffers from the amplifier's gain dependency on the output impedance of the input signal source. Moreover, they used a single-ended configuration, which makes the amplifier sensible to common-mode input voltages. In our work, we address the first issue by isolating the input during the amplification period; and the second issue by implementing the amplifier in a differential configuration.

We validated the IA performance by two-electrode ECG signal acquisition. ECG was chosen since it is one of the most demanded measurement used for diagnosing several disorders [11], [12]. Moreover, portable ECG systems are always used as a reference point in terms of how much autonomy a medical acquisition system is able to achieve [13], [14]. Particularly, two-electrode ECG measurement is attractive because of easier patient attachment (portability), patient's comfort, and lower electrode costs, to cite some reasons.

The rest of the paper is organized as follows. An analog front-end for biopotential signals acquisition is presented in Section II. Section III shows the IA architecture and its input stage is described in detail. Section IV presents the concept of the variable gain amplifier controlled by duty-cycle and its architecture with the proposed modifications. The AGC circuit implementation is also described. Measurement results of VGA and the IA applied to two-electrodes ECG measurement are shown in Section V. Finally, some conclusions are drawn in Section VI.

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II. Analog front-end

The block diagram of an AFE suitable for biopotential signals acquisition is depicted in Fig. 1. The AFE is composed of an instrumentation amplifier, a low-pass filter, a Peak-to-peak Detector (PD) and a microcontroller (uC).

The instrumentation amplifier receives the input signal from the human-body/electrodes interface. The output signal of the IA is low-pass filtered and delivered to the ADC. In order to adjust the gain of the VGA, an AGC loop is implemented by a peak-to-peak detector (PD), which delivers the signal amplitude to the uC. The latter generates the digital signals required by the IA for control of its gain.

III. Variable-gain Instrumentation amplifier

As seen in Fig. 1, the IA is composed by two main blocks: the input stage and the duty-cycle controlled VGA. Following the first one is detailed.

A. The input stage

The input stage was added mainly due to the fact that, in order to perform a two-electrode measurement, there must be a control of the large common-mode signal coupled to the body from the $50/60\,\mathrm{Hz}$ power line, since no reference electrode is used [15]. A possible saturation of the IA could happen, depending on the voltage supply, even with a high CMRR.

The amplification of the input stage was implemented by the standard front-end used in the three-operational-amplifier (OPAMP) instrumentation amplifier configuration, as Fig. 2 shows. The OPAMPs $\mathrm{X_a}$, $\mathrm{X_b}$ and resistors R_1 and R_2 provide a theoretical gain of $1 + 2\frac{R_2}{R_1}$ [16]. For the common-mode signal control, the technique of reducing the AFE's input common-mode impedance seen by the human-body/electrodes interface was considered [17], [18]. The solution implemented in [17] is simple and low-cost, so our circuit was based on it. The implementation consists on the high-pass filter formed by C_P and R_P, and on the OPAMPs $\mathrm{X_c}$ and $\mathrm{X_d}$. The high-pass filter is used for eliminating the DC components due to, in this particularly case, the half-cell potentials which are always present in ECG measurement and are not in the band of interest [1]. In a three-electrode measurement, the point between the input resistors (R_P) is connected to analog ground. In contrast, our solution senses the input common-mode signal at the mid-point of R_1 by means of a unity-gain buffer ($\mathrm{X_c}$). Then, this signal is amplified by $\mathrm{X_d}$ with a high negative gain and fedback to the common-mode node of the high-pass filter (between both R_P). As a result, the input common-mode impedance seen by the input signal is reduced.

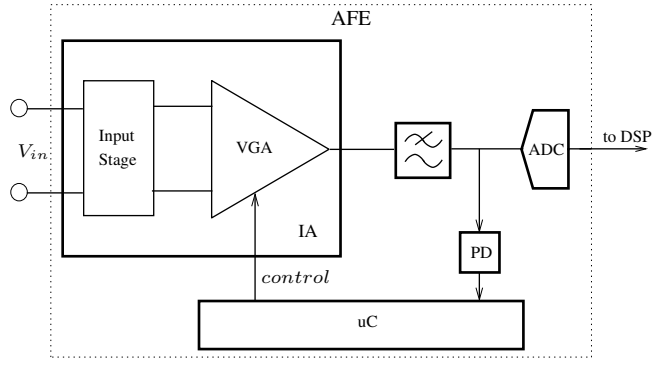

Fig. 1. Block diagram of an AFE suitable for two-electrode biopotential signal measurement.

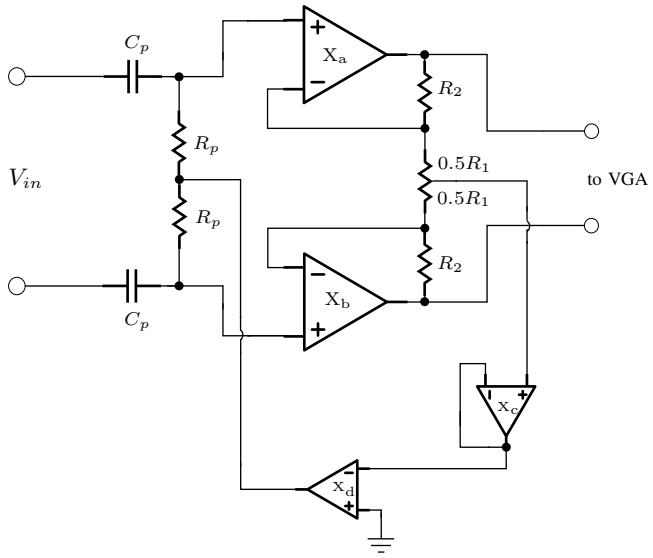

Fig. 2. Input stage of the instrumentation amplifier with control of the common-mode input signal.

IV. Variable gain amplifier controlled by duty-cycle

The concept of the VGA represented in Fig. 3(a), is based on the baseband superregenerative amplifier presented in [10], [19]. The input signal ($V_{in}(t)$) is periodically connected to the amplifier, represented by C_A and R_l. Assuming the switch turned off, the transfer function of the circuit can be expressed as:

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{1}{R_G C_A}\left(\frac{1}{s + \frac{1}{RC_A}}\right) \tag{1}$$

where :

$$R = R_G // R_l \tag{2}$$

If the transfer function (1) has a pole in the right-half plane, the circuit is said to be unstable. Considering the capacitor value as always being positive, this condition holds for a negative value of R. If R_l is negative and has an absolute value lower than R_G, this situation is attained. In the time domain, the circuit responds as follows: First, the capacitor is discharged by turning the switch on. Then, the switch is turned off and the input is connected to the amplifier. If the instability situation is given, the output will be an exponential growing voltage, which can be expressed by [10]:

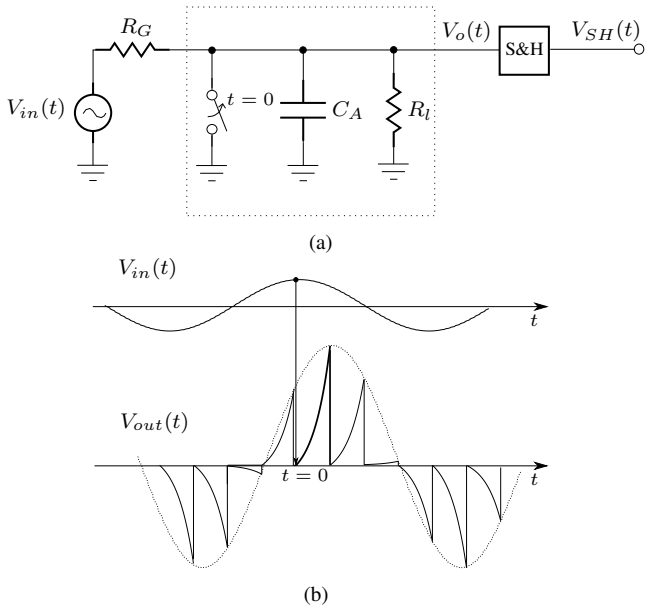

Fig. 3. Superregenerative amplifier concept (a) and a typical output waveform (b), adapted from [10].

$$V_o(t) = \frac{R_l}{R_G} V_{in}(t) \left(e^{-\frac{t}{\tau}}\right) \tag{3}$$

where τ is the time constant of the system and is given by:

$$\tau = RC_A \tag{4}$$

This time constant is negative, explaining the exponential growth in (3). A typical output waveform of the amplifier is depicted in Fig. 3(b). Each time the switch opens, the amplification takes course until it is stopped by closing the switch again, therefore, periodic exponential pulses can be observed. The amplification depends on the duration the switch remains open and, as it can be noticed, the signal can achieve large values due to the exponential dependence on this time. By adding a sample-and-hold circuit working at the end of each pulse and passing the sampled signal through a smoothing filter, a final amplified version of the input signal is obtained.

In [10], the authors synthesize the negative resistance R_l with an OPAMP connected as non-inverting amplifier with gain magnitude of 2 and with an additional resistor in positive feedback which determines the value of R_l. The proposed amplifier in our work uses the same principle for implementing R_l, though, some modifications were done, as revealed in Fig. 4. In this new arrangement, more switches (all controlled by the uC) are included with the purpose of improving two main issues: First, the input signal is sampled in a differential configuration, which ideally eliminates the input common-mode signal and makes the CMRR tend theoretically to infinite.

The other improvement implemented on this circuit is that the sampling and amplification phases are performed separately, making the gain independant of the input source

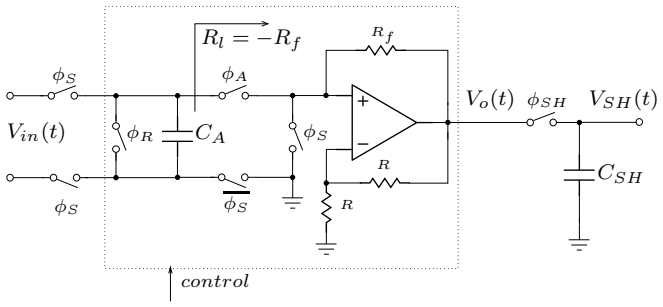

Fig. 4. Proposed circuit for the variable gain amplifier.

impedance, so the time response for this circuit is now expressed by (5), where V_i is the signal sampled at the capacitor C_A at the moment the amplification starts. It is important to notice that τ is now only defined by R_l, neglecting the effect of R_G.

$$V_o(t) = V_i \left(e^{-\frac{t}{\tau}}\right) \tag{5}$$

The proposed VGA has three operating phases, as depicted in Fig. 5. In the reset phase (ϕ_R), both terminals of C_A are shorted to analog ground. Then, the sampling period (ϕ_S) is enabled, and the capacitor is charged to the input signal. After this, the amplification starts (ϕ_A), so the capacitor is connected to the negative resistor. As a result, the sampled voltage in the capacitor is exponentially amplified until the amplification signal is disabled. As mentioned before, the sample-and-hold circuit acts at the end of the amplification period (ϕ_{SH}), and then, filtering is needed in order to reconstruct the output signal.

Recalling (5), the amplifier gain depends on the ratio between the amplification signal pulse-width (T_A) and the time constant of the circuit. Since this constant is fixed by the circuit components, the gain is controlled by the *duty-cycle* of ϕ_A. Thus, the VGA gain is given by:

$$G(T_A) = e^{-\frac{T_A}{\tau}} \tag{6}$$

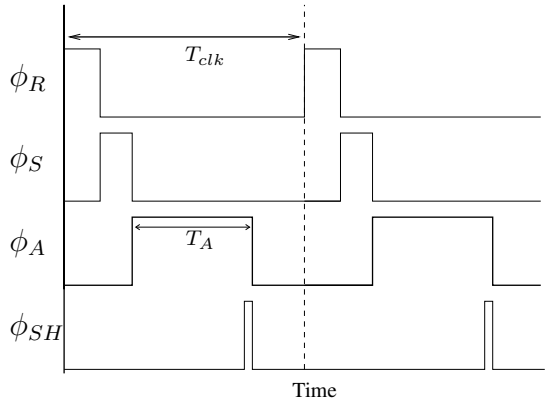

Fig. 5. Control signals for the VGA

A. Automatic gain control

The PD circuit (see Fig. 1) consists in one positive and one negative peak detectors in order to obtain the peak-to-peak amplitude of the IA output signal. Each peak detector is implemented by using a super-diode and a load capacitor [20]. A resistor is also placed in parallel with the capacitor to control the discharge time in order to match it to the input signal frequency band. The PD drives the analog input port of the microcontroller. Then, it evaluates the voltage magnitude, compares it to a reference, and provides a digital clock signal, which corresponds to ϕ_A in the VGA, with an adjusted duty-cycle in order to achieve the desired amplitude.

V. Measurement results

A. VGA

The circuit of Fig. 4 was implemented using the low-offset OP07 OPAMP and quad bilateral HCF4066B switches. In order to validate the gain expression in (6), a plot of gain versus the duty-cycle, which is defined as $\frac{T_A}{T_{clk}}$, was obtained (see Fig. 6). For this measurement, a capacitor C_A of $10\,\mathrm{nF}$ and a resistor R_f of $2.2\,\mathrm{k\Omega}$ were used. All the clock signals were fixed to $1\,\mathrm{kHz}$ and were obtained from an ATmega8 microcontroller running at $8\,\mathrm{MHz}$. The input signal was set to $2\,\mathrm{mV_{pp}}$ and $10\,\mathrm{Hz}$. From the measured gains, a fit curve based on (6) was plotted, as seen in Fig. 6. A τ of $22\,\mu\mathrm{s}$ was estimated, which is in accordance with the component tolerances and also considering the $100\,\Omega$ on-resistance value of the switches. Some deviation of the curve is observed at higher gains, which is associated to distortion caused by OP07 dynamic range.

The common-mode gain of the VGA was measured by applying a $4\,\mathrm{V_{pp}}$ $60\,\mathrm{Hz}$ common-mode signal and measuring its output while varying the duty-cycle of the control signal from 20% to 80%. From the measured common-mode gain, the calculated CMRR was $52\,\mathrm{dB}$. This value is not as high as expected from the differential configuration, and a further analysis considering the off-resistances of the switches must be done.

B. ECG measurement

The high-pass cut-off frequency of the IA input stage was chosen to be around $0.2\,\mathrm{Hz}$, with R_P of $10\,\mathrm{M\Omega}$, which is much higher than the maximum expected electrode impedance of $100\,\mathrm{k\Omega}$. For the $\mathrm{X_{a-d}}$ OPAMPs, the quad TL084 OPAMP was used. The gain in the input stage was fixed to $26\,\mathrm{V/V}$ ($28.2\,\mathrm{dB}$). A precision multi-turn potentiometer was included in series with one of the R_2 resistors in order to improve resistors matching. For the VGA, the clock frequency was fixed to $8.5\,\mathrm{kHz}$ and τ was maintained in $22\,\mu\mathrm{s}$. The sampling time of the amplification capacitor C_A was set to $20\,\mu\mathrm{s}$, long enough to ensure a correct sampling of the input signal considering the low output impedance of the OP07.

The CMRR of the complete IA was measured by applying a $4\,\mathrm{V_{pp}}$ $60\,\mathrm{Hz}$ input with both inputs shorted. It was measured for several differential gain setups and varying the input frequency from $10\,\mathrm{Hz}$ to $4\,\mathrm{kHz}$, obtaining a mean CMRR value of $72\,\mathrm{dB}$ with a $2\,\mathrm{dB}$ deviation. From the previous VGA's characterization, the expected CMRR of the IA was of $80.2\,\mathrm{dB}$, as derived from the following equation [16]:

$$CMRR_{IA} = Gain_I\,(CMRR_{VGA}) \tag{7}$$

where $Gain_I$ is the gain provided by the input stage. However, the CMRR of the TL084 OPAMPs limited the result (minimum value is $70\,\mathrm{dB}$ according to datasheet).

For two-electrode ECG measurement the period of the gain control signal was set to $20\,\mu\mathrm{s}$, which translates to an approximated gain of $30\,\mathrm{V/V}$. The output signal of the IA was passed through a 4th-order active low-pass filter with its cut-off frequency in $100\,\mathrm{Hz}$. The measured ECG wave presented a visible $60\,\mathrm{Hz}$ component, however, the control of the input-common mode signal by the reduction of the input common-mode impedance was successfully achieved without saturating the IA. A digital notch filter at $60\,\mathrm{Hz}$ was applied as

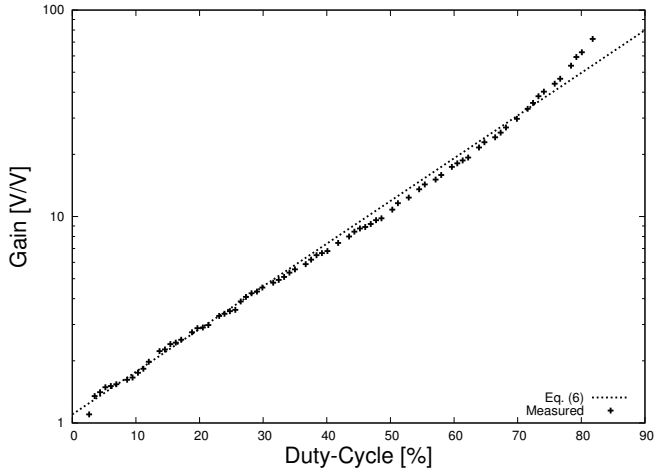

Fig. 6. Gain of the VGA vs duty-cycle of the digital clock control signal

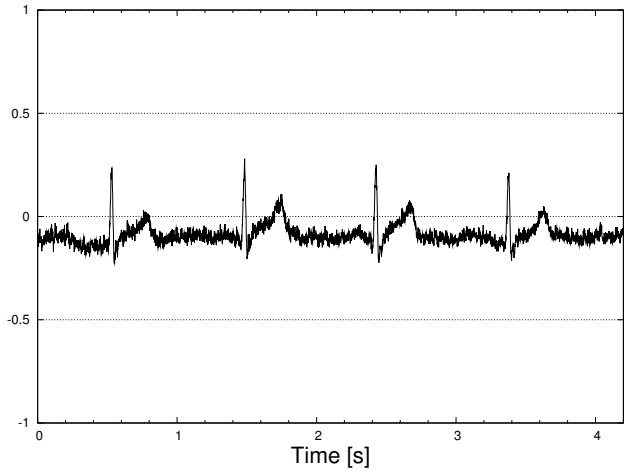

Fig. 7. Two-electrode ECG measurement.

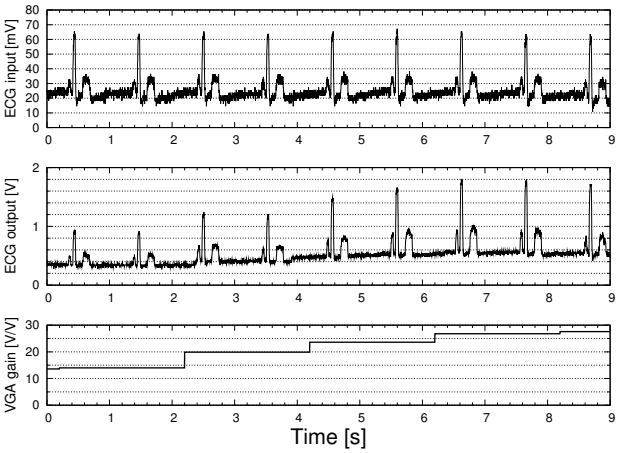

Fig. 8. Automatic Gain Control for the ECG waveform.

a post-processing step of the ECG signal and shown in Fig. 7. This results proves that the implemented front-end allows the acquisition of two-electrode ECG signal for further processing executed either on-line (e.g. in the uC) or off-line. Two $9\,\mathrm{V}$ batteries were used to obtained the regulated $\pm 5\,\mathrm{V}$ supply for the analog front-end circuits. The ECG measurement was performed for standard lead-2 configuration using Ag/AgCl electrodes and shielded twisted cables.

A test for the dynamic response of the IA to the AGC circuit was also performed in which a $2\,\mathrm{mV_{pp}}$ ECG generator circuit was used as input signal for simplicity. The performance of the circuit is shown in Fig. 8. The ECG input signal after the input stage is shown on top. Its amplitude is of approximately $50\,\mathrm{mV_{pp}}$ provided the fixed gain of $26\,\mathrm{V/V}$ in this stage. The output signal is shown on the middle, where the amplification of the ECG wave in time can be observed. It stabilizes until the amplitude reaches a value between 1.3 and $1.4\,\mathrm{V}$, since these values were set in the uC. A plot of the equivalent VGA's gain, proportional to the duty-cycle of the control signal, is presented on the bottom. The ECG signal is periodically evaluated within a time window which considers the time constant of discharge of the peak-to-peak detector, which was set around 1 second for this test.

VI. Conclusions

An instrumentation amplifier for biomedical signal acquisition with duty-cycle controlled gain based on the superregenerative concept was presented. This digital gain control makes this circuit a suitable alternative against common VGAs and PGAs due to its easy gain setting that dispenses with a D/A converter while preserving a high gain-step resolution. A prototype of the IA using discrete components was implemented. The measured gain range of the VGA was $40\,\mathrm{dB}$ with a gain step resolution of $0.5\,\mathrm{dB}$. Its variable gain performance was tested using a ECG generator and an a AGC circuit implemented by a peak-to-peak detector and a microcontroller. The IA amplifies the ECG input signal of $2\,\mathrm{mV_{pp}}$ until the desired range between 1.3 and $1.4\,\mathrm{V}$ in no more than 6 ECG-wave R-peaks. Finally, the IA was tested by performing a two-electrode ECG measurement. Results showed that the input stage of the IA effectively controls the input-common mode voltage range caused by the power line interference without using a third electrode as ground reference.

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