A 25-dBm 1-GHz Power Amplifier Integrated in CMOS 180nm for Wireless Power Transferring

Fabian L. Cabrera, and F. Rangel de Sousa
Radiofrequency Laboratory
Federal University of Santa Catarina
Florianópolis-SC, 88040-900, Brazil.
fabian.l.c@ieee.org, rangel@ieee.org

ABSTRACT

This paper presents the design of a power amplifier integrated in a CMOS 180 nm technology, which is intended to drive an inductive link operating at 990 MHz. A class-D topology is employed to avoid the use of inductors. A design methodology is proposed to find the optimal transistor width, solving the trade-off between the ON-resistance and gate capacitance. The area occupied is 1.5 mm^2, most of it is used by the PADs and the wide interconnects. Post-layout simulations showed a power efficiency of 58% when delivering 25.1 dBm to the primary inductor of a wireless power transferring system.

Categories and Subject Descriptors

B.7.0 [**Integrated Circuits**]: General – advanced.

General Terms

Theory

Keywords

Class-D, CMOS, integrated circuits, power amplifier, power efficiency, wireless power transfer.

1. INTRODUCTION

Miniaturized electronic devices may have a reduced volume by avoiding bulky batteries. Instead of that, those devices can be remotely powered by using wireless power transferring (WPT). The WPT systems are typically implemented with inductive links, where the energy is transferred through magnetic coupling between two inductors: the primary inductor is connected to the source and the secondary inductor is embedded into the miniaturized device. The WPT system can be summarized as shown in Fig. 1(a). The source and the load operate at DC, while the inductive link needs an RF signal whose frequency must be chosen to optimize the link efficiency [1]. As a consequence, a DC-to-RF converter is necessary to supply energy to the link and other block is necessary after the link for the inverse process. A common way to do the DC-to-RF conversion is by using an oscillator connected to a power amplifier (PA) as shown in Fig. 1(b). Since the PA has to deliver relatively high power levels to the inductive link while achieving high energy efficiency, its design constitutes a challenge to the WPT system development.

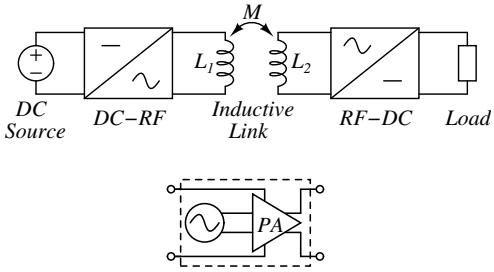

Figure 1: (a) WPT system summary. (b) DC-RF implementing.

With respect to the discrete PA, CMOS integrated power amplifiers have important advantages, such as reconfigurability, reduced area, lower cost and higher reliability. Most of the integrated PA use switched topologies such as class-D [2] and class-E [3–8]. The popularity of the class-E topology comes from the high efficiency achieved in its discrete implementation (up to 90%). In that case, single-stage class-E amplifiers are also preferred because they can be implemented with only one transistor. On the other hand, integrated PA can be differential to combine the power of two output stages. For example, in [8] a differential class-E PA with CMOS integrated transistors was implemented and a power added efficiency (PAE) of 70.7% at the output power of 29 dBm was measured. The efficiency is still high, partly because the passive components (capacitors and inductors) are located off-chip and therefore they may have a good quality factor. Class-E amplifiers require at least one RF-choke inductor (or two for differential amplifiers) which are difficult to integrate. This is because CMOS integrated inductors are very lossy and occupy a large portion of the chip area. An intermediate solution is to use bondwire inductances [3–6]. However, the value of bondwire inductances are limited and are not well controlled.

Class-D integrated amplifiers are based on complementary NMOS and PMOS switches, thus they do not require the choke inductor. For that reason they are better suitable for CMOS integration. Furthermore, they have a wideband characteristic since they do not contain resonant circuits. Taking advantage of this feature, in [2] a class-D differential amplifier was designed with measured efficiency of 55% and 45% at the frequencies 900 MHz and 2.4 GHz respectively. Although the PA core in [2] is integrated, the effi-

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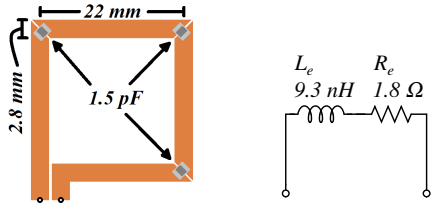

Figure 2: (a) Primary inductor. (b) Equivalent impedance at 990 MHz.

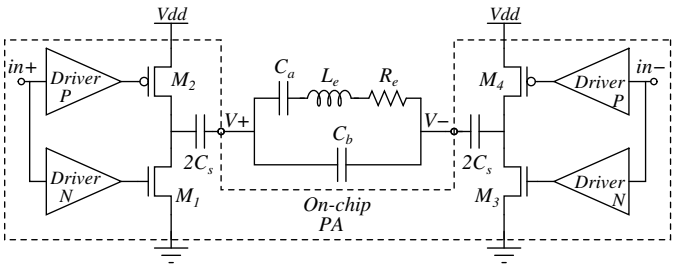

Figure 3: PA topology.

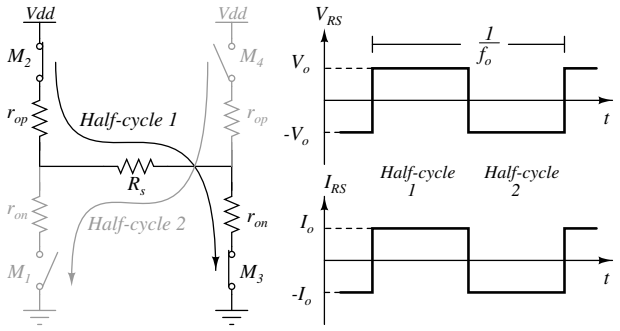

Figure 4: (a) Power amplifier model. (b) Model voltage and current waves.

ciency was boosted by using external third-harmonic LC filters.

In this work we develope a methodology for designing a CMOS class-D PA used to drive an inductive link. The proposed methodology solves the trade-off between ON-resistance and gate capacitance of the switches, resulting in the optimal choice of the driving transistors width. The equations presented allow the calculation of the value of all the circuit components including the capacitors used for impedance transformation. The design procedure is explained in the next section. In section III we present the circuit implementation, the layout considerations and the post-layout simulation results. Finally, the conclusions are drawn in section IV.

2. DESIGN

2.1 Specifications

The PA proposed is intended to drive an inductive link whose primary inductor is printed on a FR4 board with the dimensions shown in Fig. 2(a). The secondary side is a fully integrated wireless power receiver with a measured resonant frequency of 990 MHz [9, 10]. The power delivered to the primary inductor was specified to be 25 dBm. The inductive link is expected to operate under the weak coupling regime, for this reason the input impedance is approximately the impedance of the primary inductor. The equivalent impedance of the inductor of Fig. 2(a) was obtained from full-wave electromagnetic simulation performed in the software EMPRO® from Keysight®, its value at the frequency of interest is $Z_e|_{f=990e6} = 1.77 + j57.8$. This impedance can be represented with an inductor in series with a resistor as shown in Fig. 2(b).

2.2 Topology

The diagram of the differential class-D PA is shown in Fig. 3. The transistors M_1 to M_4 act as switches. The drivers are necessary since the gate capacitance is high, given that the transistors width is in the order of mm. The driver N is different from the driver P to guarantee the slow turn-on and the fast turn-off of the switches. In that way, the direct path between V_{dd} and ground is avoided during transitions. The PA load is the primary inductor of the inductive link represented by L_e and R_e. The capacitors C_s, C_a and C_b form the so called impedance transformation network. The capacitor C_a must be off-chip because the voltage at the terminals of the inductor can exceed the permitted values for the chip components. On the other hand, the choice of the C_s integration has at least two advantages: 1) low harmonics level at the chip output, which translates into lower power losses. 2) higher output voltage, which means a reduction in the output current for the same power level and hence lower losses in the wirebond parasitic resistance. The output PAD and wirebond capacitances can be included into the capacitor C_b. Although the C_b capacitance could be fully integrated, we decided to implement it externally to provide more flexibility to the design.

The model of Fig. 4(a) can be used to understand the operation of the PA. Each transistor is represented by an ideal switch and a series resistance: r_{on} for the NMOS transistor and r_{op} for the PMOS case. The load impedance is transformed by C_a, C_b and C_s into the resistance R_s at the frequency of interest f_o. Supposing control signals at f_o with ideal transitions and duty cycle of 50%, the waves corresponding to the voltage (V_{RS}) and the current (I_{RS}) across R_s are drawn in Fig. 4(b). The switches M_1 and M_4 are open in the first half-cycle of the control signal, while M_2 and M_3 are closed. The magnitude of the current (I_o) and the voltage (V_o) across R_s are expressed by (1) and (2) respectively. In the second half-cycle all the switches change their states inverting the sign of V_{RS} and I_{RS}.

$$I_o = \frac{V_{dd}}{R_s + r_{on} + r_{op}} \tag{1}$$

$$V_o = \frac{V_{dd} R_s}{R_s + r_{on} + r_{op}}. \tag{2}$$

The power drawn from the DC supply can be calculated by multiplying V_{dd} and the current in (1):

$$P_{DC} = V_{dd} I_o = \frac{V_{dd}^2}{R_s + r_{on} + r_{op}}. \tag{3}$$

The power delivered to the load is the power consumed by R_s at the fundamental frequency ($P_{Rs(1)}$). Only the fundamental frequency is considered due to the bandpass nature of the capacitive network combined with the inductor. The $P_{Rs(1)}$ value is given by:

$$P_{Rs(1)} = \frac{1}{2}\left(\frac{4V_o}{\pi}\right)\left(\frac{4I_o}{\pi}\right) = \frac{8V_{dd}^2 R_s}{\pi^2 (R_s + r_{on} + r_{op})^2}, \tag{4}$$

where the factor $\left(\frac{4}{\pi}\right)$ corresponds to the fundamental component

of the voltage and the current waves of Fig. 4(b) respectively. In practice, the I_{Rs} current waveform is not completely squared because the equivalent impedance for the third and higher harmonics is not R_s anymore. However, the approximation done in the model of Fig. 4 is sufficient to describe the PA behavior.

The required value of R_s can be solved from (4):

$$R_s = \frac{4V_{dd}^2}{\pi^2 P_{Rs(1)}} \left(1+\sqrt{1-\frac{\pi^2 P_{Rs(1)}(r_{on}+r_{op})}{2V_{dd}^2}}\right) - (r_{on}+r_{op}). \tag{5}$$

The expression in parentheses of the first term in (5) has the form of $1+\sqrt{1-x}$ which can be approximated to $2-\frac{x}{2}$ for x values near to zero. Then the R_s value can be approximated by:

$$R_s \approx \frac{8V_{dd}^2}{\pi^2 P_{Rs(1)}} - 2(r_{on}+r_{op}). \tag{6}$$

The power efficiency η can be defined as:

$$\eta = \frac{P_{Rs(1)}}{P_{DC}+P_{drive}}, \tag{7}$$

where P_{drive} is the power used by the drivers to charge the gate capacitance (C_g) of the switches and it is given by:

$$P_{drive} = C_g V_{dd}^2 f_o, \tag{8}$$

where $C_g = 1.5(2C_{gp}+2C_{gn})$; C_{gp} and C_{gn} are the PMOS and NMOS gate capacitances respectively. The factor 1.5 is used to indicate the capacitance excess due to the driver implementation. Using (3), (4) and (8) into (7), we can obtain an expression for the efficiency:

$$\eta = \frac{1}{\frac{\pi^2}{8} + \frac{\pi^2(r_{on}+r_{op})}{8R_s} + \frac{C_g V_{dd}^2 f_o}{P_{Rs(1)}}}. \tag{9}$$

2.3 Sizing the transistors

Equation (9) shows the dependence of the efficiency with the ON-resistance and gate capacitance of the transistors, which can be modeled with (10) and (11) respectively:

$$r_{on}+r_{op} = \frac{a}{W} \tag{10}$$

$$C_g = bW, \tag{11}$$

where a and b are parameters obtained from simulations; and W is the transistors width. Both PMOS and NMOS transistors are assumed to have the same width even though r_{op} is greater than r_{on}. An attempt to equate r_{op} to r_{on} would lead to wider PMOS transistors increasing the gate capacitance. The V_{dd} value is chosen to be 1.8 V which is the nominal voltage of the regular transistor of the CMOS 180 nm technology. The length of all transistors is set to its minimal value of 180 nm. Through simulations made in the software Cadence® we found a value of 7.8 nF/m for the parameter b. The normalized ON-resistance of the PMOS and the NMOS transistors is plotted in Fig. 5 as function of the drain-to-source voltages $|V_{dsp}|$ and V_{dsn} respectively. Initial values for $|V_{dsp}|$ and V_{dsn} must be guessed to calculate a. For example, we can suppose an initial value of 0.3 V for $|V_{dsp}|$ and 0.1 V for V_{dsn} which results in a value of 4.6 mΩ.m for the parameter a.

By replacing (10) and (11) into (9) and rearranging the terms we can find an expression for the reciprocal of efficiency:

$$\frac{1}{\eta} = \frac{\pi^2}{8} + \frac{\pi^2}{8}\frac{1}{\left(\frac{8V_{dd}^2 W}{\pi^2 a P_{Rs(1)}} - 2\right)} + \frac{bWV_{dd}^2 f_o}{P_{Rs(1)}} \tag{12}$$

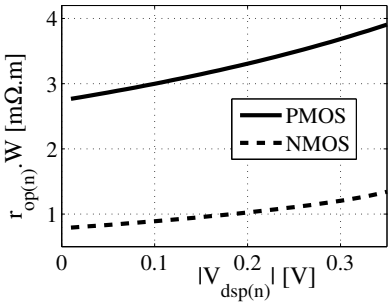

Figure 5: Transistors ON resistance as function of the drain-to-source voltage.

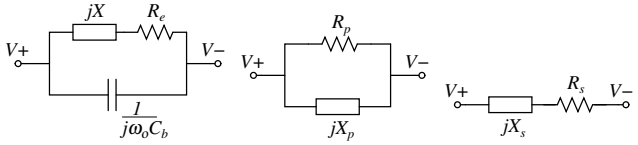

Figure 6: Equivalent impedance: (a) First simplification. (b) Parallel. (c) Series.

Equation (12) is a function of W which has a point of minimum thus maximizing the efficiency. This point corresponds to the optimal width and can be calculated as:

$$W_{opt} = \frac{\pi^2 a P_{Rs(1)}}{8V_{dd}^2}\left(\frac{1}{\sqrt{abf_o}}+2\right). \tag{13}$$

The maximum efficiency η_{max} can be calculated by doing $W = W_{opt}$ in (12), resulting in (14).

$$\frac{1}{\eta_{max}} = \frac{\pi^2}{8}\left(1+2\sqrt{abf_o}+2abf_o\right) \tag{14}$$

According to (14) the maximum efficiency only depends on the technology characteristics a and b, and on the frequency. To achieve that efficiency R_s must be equated to its optimal value R_{sopt}, which can be calculated from (6), (10) and (13):

$$R_{sopt} = \frac{8V_{dd}^2}{\pi^2 P_{Rs(1)}}\left(\frac{1}{1+2\sqrt{abf_o}}\right) \tag{15}$$

2.4 Impedance transformation network

The calculation of the components of the impedance transformation network can be done by simplifying the circuit of Fig. 3 between the nodes $V+$ and $V-$. The first simplification can be seen in Fig. 6(a) where the L_e and C_a reactances are added at the angular frequency $\omega_o = 2\pi f_o$. The resulting reactance X is given by:

$$X = \omega_o L_e - \frac{1}{\omega_o C_a}. \tag{16}$$

The impedance of Fig. 6(a) can be further simplified to the parallel circuit of Fig. 6(b) or to the series circuit of Fig. 6(c). In the series equivalent appears the resistance R_s which is the same used in the PA model, therefore the reactance jX_s must be canceled with the series capacitor impedance $-j/(\omega_o C_s)$. The parallel equivalent resistance R_p must be chosen to not exceeding the voltage limits of each integrated capacitor of value $2C_s$. The R_p value is calculated

as:

$$R_p = \frac{V_H^2}{2P_{Rs(1)}}, \tag{17}$$

where V_H is the peak-to-peak voltage allowed in each differential output node $V+$ and $V-$. According to the manufacturer, the output nodes can tolerate voltages of ± 5 V, thus allowing a peak-to-peak voltage of 10 V in each node. The value of V_H used to the PA design was 9 V. The equivalent admittance (Y) of the circuit of Fig. 6(a) is given by:

$$Y = \frac{R_e}{R_e^2 + X^2} + j\left(\omega_o C_b - \frac{X}{R_e^2 + X^2}\right). \tag{18}$$

The real part of Y must be equal to $1/R_p$, therefore we can calculate X as expressed in (19). Using (16) and (19) is possible to find the C_a value:

$$X = \sqrt{R_e(R_p - R_e)} \tag{19}$$

$$C_a = \frac{1}{\omega_o(\omega_o L_e - \sqrt{R_e(R_p - R_e)})}. \tag{20}$$

On the other hand, the equivalent impedance is the reciprocal of Y as shown in (21). The capacitance C_b can be solved after equating the real part of Z to R_s:

$$Z = \frac{1}{Y} = \frac{R_e + j(X - \omega_o C_b X^2 - \omega_o C_b R_e^2)}{(1 - \omega_o C_b X)^2 + (\omega_o C_b R_e)^2} \tag{21}$$

$$C_b = \frac{1}{\omega_o R_p}\left(\sqrt{\frac{R_p}{R_e} - 1} - \sqrt{\frac{R_p}{R_s} - 1}\right). \tag{22}$$

The value of X_s and hence C_s can be calculated from the equivalence between the circuits of Fig. 6(b) and Fig. 6(c), resulting in:

$$C_s = \frac{1}{\omega_o\sqrt{R_s(R_p - R_s)}} \tag{23}$$

2.5 Design Methodology

The design methodology can be summarized in the next steps:

1. The PA design starts from the specifications $P_{Rs(1)}$, f_o and the load R_e and L_e. It is also important to know the technological constraints as V_{dd} and V_H.

2. Calculate the value of R_p using (17).

3. Simulate PMOS and NMOS transistors to obtain the parameter b and the curves of $(r_{op}W)$ and $(r_{on}W)$ as shown in Fig. 5.

4. Estimate from the curves of Fig. 5 the values of the parameter a, assuming a value for $|V_{dsp}|$ and for V_{dsn}.

5. Calculate the optimal values for the transistor width W_{opt} and for the equivalent resistance R_{sopt} by using (13) and (15) respectively.

6. Find $|V_{dsp}| = I_o r_{op}$ and $V_{dsn} = I_o r_{on}$ by replacing W_{opt} and R_{sopt} into (10) and (1). With the updated values of $|V_{dsp}|$ and V_{dsn} repeat steps 4) to 6) until the value of a does not change significantly.

7. Calculate the capacitances C_a, C_b and C_s from (20), (22) and (23) respectively.

Table 1: Numeric results of the design methodology.

1	$P_{Rs(1)}$	316	mW	4	a	4.3	mΩ.m
	f_o	990	MHz	5	W_{opt}	3.9	mm
	R_e	1.8	Ω		R_{sopt}	6.1	Ω
	L_e	9.3	nH	6	$\|V_{dsp}\|$	220	mV
	V_{dd}	1.8	V		V_{dsn}	54	mV
	V_H	9	V	7	C_s	5.9	pF
2	R_p	128.1	Ω		C_a	3.8	pF
3	b	7.8	nF/m		C_b	4.9	pF

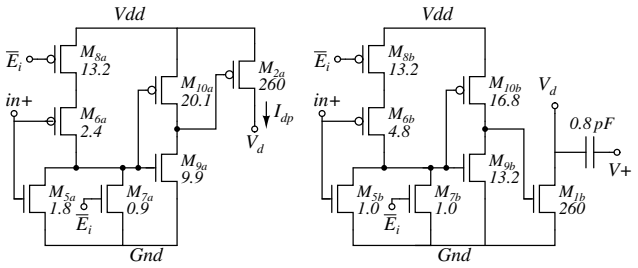

Figure 7: PA unit cell: (a) PMOS part. (b) NMOS part.

The equations presented for the impedance transformation network assume that R_p is greater than R_e and that R_p is greater than R_s. If one of these conditions is not true, the network configuration must be redefined. The design methodology was executed, the results are shown in table 1. Initially it was assumed that $|V_{dsp}|$ was 0.3 V and that V_{dsn} was 0.1 V corresponding to a value of 4.6 mΩ.m for a. In the second iteration the value of a was corrected to 4.3 mΩ.m. The design procedure converged at the second iteration. The values of table 1 correspond to the second iteration. The theoretical maximum efficiency calculated from (14) is 57 %.

3. IMPLEMENTATION

3.1 Circuit implementation

The implemented circuit is based on the diagram of Fig. 3. Each transistor M_1 to M_4 was divided into 15 unit cells. Each unit cell can be enabled or disabled using a signal $\overline{E}_i$ thus providing digital control over the output power. The schematic of the PMOS and NMOS parts of the unit cell is shown in Fig. 7(a) and in Fig. 7(b) respectively. The channel length was 180 nm for all transistors and the width is indicated in the figures, the units are in μm. The transistors $M_{5a(b)}$ to $M_{10a(b)}$ were sized to drive the switches at the specified frequency considering that transitions must be slow while turning the switches on and fast while turning them off. The capacitor $2C_s$ is also divided into 15 parts, so each part of 0.8 pF is included into the unit cell as shown in Fig. 7(b). Each capacitor is integrated using the MIM (Metal-Insulator-Metal) option which provides a high quality factor.

3.2 Layout

The layout of the entire chip is shown in Fig. 8(a). In addition to the PA, the chip includes a PLL for generating the differential input signal for the PA and an envelope detector (ED) to sense the backscattered response at the inductive link (their implementation is out of the scope of this paper). The chip floorplanning is very important since the DC current through the supply nodes (Gnd and

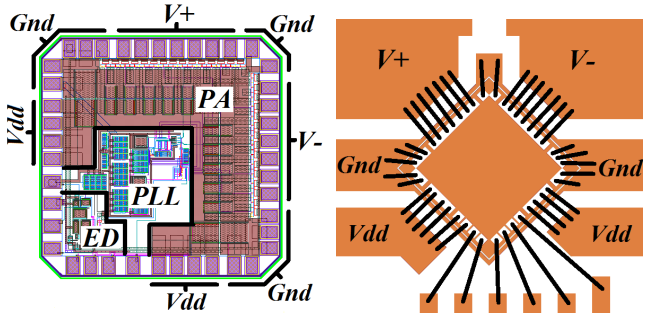

Figure 8: (a) Layout 1.5 mm × 1.5 mm. (b) PCB bonding diagram.

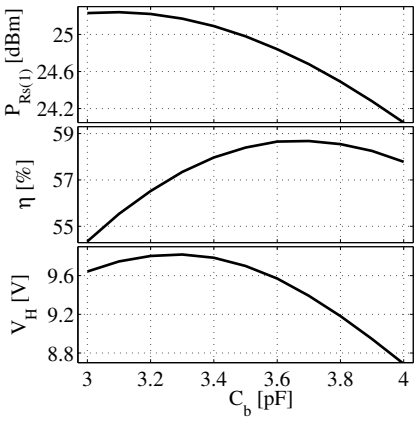

Figure 9: Output power, efficiency and voltage excursion at node V+.

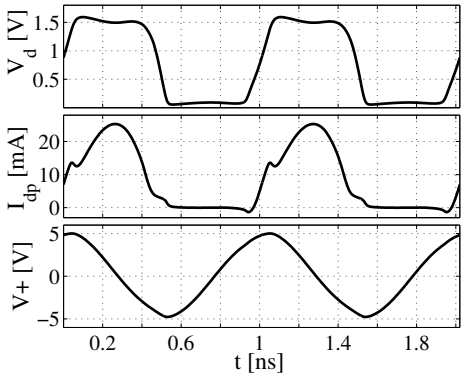

Figure 10: Time domain waveforms at one PA unit cell.

Vdd) can be up to 300 mA. For that reason, a large number of PADs was used for Gnd (12), Vdd (8), $V+$ (7) and $V-$ (7). The PADs were organized in such way to facilitate the wirebonding process to the printed board as illustrated in Fig. 8(b), where the chip appears rotated 45° counterclockwise. In this configuration, the bondwires length and the interconnections inside the chip are kept as short as possible. Each trace that connects the supply PADs to the PA unit cells has a width of 175 μm and is drawn in the thicker metal to decrease the series resistance and hence the voltage drop. Dual-MIM capacitors were included between Gnd and Vdd using the space under the wide thick metal thus filtering the supply voltage. The layout of each unit cell occupies an area of only 60 μm × 55 μm. They are positioned in a row behind the output PADs, in that way the current from the supply traces and delivered to output PADs is well distributed.

3.3 Results

The circuit and the parasitic resistances and capacitances were extracted from the layout. Post-layout simulations were done in the Cadence® environtment. The off-chip capacitor C_a and the load values are those informed in Table 1. The C_b value must be significantly lower than the value calculated in Table 1 because the PAD capacitance must be subtracted. The simulations results when sweeping the C_b value are shown in Fig. 9. An output power of 25.1 dBm is achieved with an efficiency of 58% when C_b=3.4 pF, which is near to the maximum efficiency point. The output voltage excursion at C_b=3.4 pF is 9.8 V, which is below the specified limit. From Fig. 9 we can infer the PA performance variation due to the resolution in the discrete capacitors value, the resolution for the available capacitors is 0.1 pF. According to the figure, a value of 3.4±0.1 pF for C_b results on the output power of 25.1∓0.1 dBm with efficiency of 58%±0.6%.

The time domain signals at one PA unit cell are shown in Fig. 10 for C_b=3.4 pF. V_d is the drain voltage at the switches and I_{dp} is the PMOS drain current as marked in Fig. 7(a). The voltage waveform is squared as expected in the PA model. The voltage drop $|V_{dsp}|$ when the PMOS transistor is turned-on is near the predicted value of 220 mV. On the other half-cycle, the NMOS voltage drop V_{dsn} is near the calculated value of 54 mV. The I_{dp} current waveform presents less similarity with the squared form. However, its peak value is near the calculated fundamental frequency component $\left(\frac{4I_o}{\pi}.\frac{1}{15}\right)$ which corresponds to 21.3 mA. Another wave shown in Fig. 10 is the voltage at one of the differential output nodes ($V+$). The wave has a sine form with voltage excursion between -5 V and 5 V approximately.

Additional simulations were done by sweeping the number (N) of enabled PA cells. The results are shown in Fig. 11. The curve with circled marks corresponds to the configuration optimized for N=15 (C_a=3.8 pF and C_b=3.4 pF). In that configuration, the output power can be swept from 3 dBm to 25 dBm with efficiency ranging from 10% to 58% respectively. For lower N values, the efficiency can be increased by adjusting the capacitances C_a and C_b as indicated in Fig. 11. With the adjusted values, the output power is found between 5 dBm and 22 dBm with efficiency of 16% and 51% respectively. The highest N values can not be used in this configuration because the V_H value would exceed the specified limit of 10 V.

In Table 2 the results of the designed PA are compared with other CMOS integrated PAs having similar specifications. However, all the works cited have different degree of integration. The PA designed in [7] is fully integrated, it uses an on-chip transformer to combine the power of two differential output stages. Nevertheless, it has the worst efficiency and the wider silicon area among all references. On the opposite direction is the PA implemented in [8] where only the transistors were integrated; all capacitors and inductors were implemented outside the chip, which leads to the best efficiency and smaller silicon area among the compared works. In [3] the inductors are implemented with the bondwires, however bondwire inductances have limited values and suffer from large process variations.

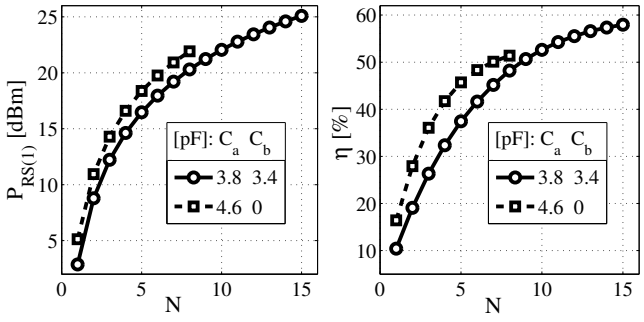

Figure 11: Sweep in the number of PA cells enabled. (a) Power. (b) Efficiency.

Table 2: Comparison of CMOS integrated PAs.

Ref.	f_o [MHz]	$P_{Rs(1)}$ [dBm]	η [%]	Area [mm^2]	Tech. [nm]	Class	Inductors
[7]	800	30.4	40.7	5	180	E	On-chip transformer
[3]	900	29.5	41	4	250	E	Bondwires
[2]	900	24.4	55	1.2	45	D	External
This work	990	25.1	58	1.5	180	D	No
[8]	820	29	70.7	0.5	180	E	External

The PA designed in this work is highly integrated, only two capacitors are left outside the chip. The efficiency achieved is the best between the references with high degree of integration. The silicon area is kept small because the PA does not use inductors. The high efficiency was obtained thanks to the design methodology proposed, which considers the trade-off between ON-resistance and gate capacitance for choosing the optimal width of the transistors.

4. CONCLUSION

A power amplifier was designed to drive an inductive link operating at 990 MHz. The class-D topology was chosen looking for high efficiency and wideband operation, while achieving high degree of integration. A design methodology is proposed to find the optimal width of the MOS transistors used as switches. The PA is integrated in an IBM CMOS 180 nm process and occupies a silicon area of 1.5 mm^2. The PA is divided into 15 unit cells allowing the individual enabling or disabling of each cell, in that way the output power can be digitally controlled. Post-layout simulations of the PA show that the maximum output power is 25.1 dBm with an efficiency of 58%.

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