Design of a Wideband LNA for Human Body Communication

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Abstract—**This paper presents the design of a LNA (Low Noise Amplifier) operating between 1-100MHz for HBC (Human Body Communications). The circuit is based in a wideband topology that exploits the principle of noise canceling, and avoids the use of inductors. It was designed in CMOS 0.18um/1.8V, consumes 10mA, has a maximum noise figure of 3.81 dB and a gain (S_{21}) of 15.58 dB. Monte Carlo and corners simulation results are presented for the post layout extraction of the design.**

Keywords— low noise amplifier, noise canceling, human body communication, wideband, inductorless.

I. INTRODUCTION

HBC is a recent technology for transmitting signals, which is based on electric field coupling to the human body [1]. The signal is fed to the body through electrodes as show in Figure 1, and is transmitted at frequencies below 100MHz [2]. Since at such low frequencies most of the signal is limited to the body, HBC has the characteristics of low interference, high security, and low power consumption [3]. Overall, these aspects make HBC specially suitable for body area networks, being presented as one of the tree PHY (physical layer) covered by the IEEE 802.15.6 standard [4].
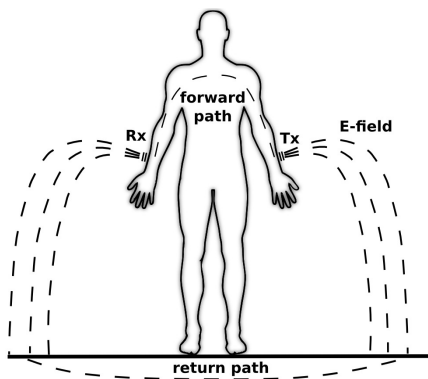

Figure 1 - Human Body communication principle.

Concerning the transceiver design, the operation at low frequency enables the use of an almost fully digital implementation for the transmitter, however in the receiver side, an analog front-end is still required [5]. The signal captured by the receiver electrodes is usually directly processed by an LNA, apart from cases where impedance matching or filtering circuits are used, which is responsible to provide considerable gain, proper matching, and to add as little noise as possible [6].

The literature regarding HBC LNA is relatively scarce. Commonly, the block design description is almost completely absent, as in [7], [8] and [9], or superficial at best, as in [10] and [11]. In [7] a parallel combination of CS (common source) and CG (common gate) stages is used, making the LNA a single-ended to differential converter, still no information is given regarding noise figure, gain, or power consumption, its only stated that the total receiver power is 2.25mW. In [8] a topology based in operational amplifiers is presented, again most of the LNA main performance metrics are omitted, the informed bandwidth is located in the lower HBC band between 0.3-15 MHz, and the power consumption is 0.76mW. In [9] a two stage LNA is proposed, achieving a gain of 38dB in the frequency band comprised between 1-30MHz, and the stated receiver power is 2.1mW. In [10] a dual band LNA based on a cascode LC topology is reported. It has noise figure of 3dB, gain of 16 dB and consumes 2.16 mW, but operates in a narrow bandwidth between 30-70MHz. In [11] a LNA with reconfigurable gain based in a cross-coupled CG amplifier is presented, the circuit has a noise figure of 3-16dB, the gain varies between 13-22dB, it operates between 40-120MHz, the authors claim its power consumption is 0.6mW. Reference [12] is the only one dedicated to a complete discussion of the design, and presents an inverter amplifier with resistor feedback that tries to achieve noise canceling. It has a noise figure of 2.5 dB, gain of 16 dB and operates in 0.1-100MHz range, but the total power consumption or efforts to minimize it are not mentioned.

Given that the presented designs do not make clear any evident trend regarding a suitable HBC LNA topology, some considerations can be made to help choosing the proper circuit: the use of narrowband circuits, such as the cascode LC topology, can lead to good noise performance, but consumes large area to achieve proper matching, and do not easily cover the desired operation band between 1-100MHz. Classical wideband topologies, such as common-gate and common-source with resistor feedback have good matching, but generally poor noise performance. An alternative is to

apply the circuit technique presented by Bruccoleri in [13] to cancel thermal noise, achieving good wideband matching and noise performance simultaneously [12], [14]. With this in mind, a topology based in the noise canceling principle will be employed.

The paper is organized as follows: Section II describes the noise canceling approach, Section III presents and discuss the LNA circuit design, Section IV analysis the simulations results, and Section VI draws some conclusions.

II. NOISE CANCELING PRINCIPLE

The concept behind the noise canceling technique [13] is to create two paths with opposite phase polarity but the same gain magnitude for the noise generated by the circuit, so that when added at the output, only the noise is canceled. Figure 2 illustrates this principle in a general form. M_1 is the input transistor and it is called the matching stage. Its generated current noise $I_{n,M1}$ appears at points X and Y with the same polarity. To achieve noise canceling, an additional amplifier, called the noise canceling stage, has to be added, and its gain A has to be set such that voltages at nodes Y and Z are equal but with opposite polarity. Note that the input signal v_i has the same polarity at nodes Y and Z, given the inverted gain of the common-source and of the noise canceling stage.
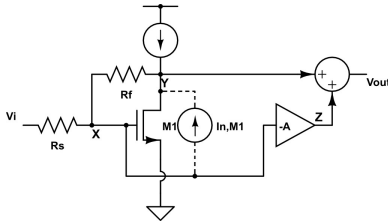

Figure 2 – Noise canceling principle.

To find the required gain A that enables the noise canceling for the matching stage, we start by modeling the noise current $I_{n,M1}$ as a source between the drain and source terminals of M_1. Then the noise voltages at X, Y, Z and at the output are respectively:

$$V_{n,X} = \alpha I_{n,M1} R_s \tag{1}$$

$$V_{n,Y} = \alpha I_{n,M1} \left(R_s + R_f \right) \tag{2}$$

$$V_{n,Z} = -A V_{n,X} = -A \alpha I_{n,M1} R_s \tag{3}$$

$$V_{n,OUT} = V_{n,Y} + V_{n,Z}$$

$$V_{n,OUT} = \alpha I_{n,M1} \left(R_s + R_f \right) - A \alpha I_{n,M1} R_s \tag{4}$$

Where R_s is the source impedance, R_f the feedback resistance, and α depends on the relationship between $Z_{in} = 1/g_{m1}$ and R_s, with g_{m1} being the transconductance of the

transistor M_1. From (4), we can easily conclude that to achieve noise canceling, the gain A has to be:

$$A = 1 + R_f / R_s \tag{5}$$

III. CIRCUIT DESCRIPTION AND DESIGN

A common circuit implementation of this technique appears in Figure 3. It uses a CMOS inverter with feedback resistor as the matching stage, a cascode amplifier as the noise canceling stage, and a source follower is placed at the output to add the signals at each path. The inverter, formed by M_{1a} and M_{1b}, improves the overall input stage transconductance. Transistor M_2 sets the gain through g_{m2}, with M_{2b} added to improve isolation and lower the input capacitance. M_3 adds the signals, provides the output impedance match and acts as load for M_2, helping to set the proper gain. R_2C_2 is a high-pass filter, providing AC coupling between the inverter and M_3, and C_1 AC-couples M_{1b} to ground. For the current sources we have: I_{BIAS1} makes the input inverter less vulnerable to supply voltage variations, and I_{BIAS2} helps to provide the proper current for M_2 without imposing the same bias current to M_3.

Analyzing the circuit in Figure 3, the following conditions have to be fulfilled for input and output matching, and noise canceling, respectively [13]:

$$R_{input} = 1/\left(g_{m1a} + g_{m1b} \right) \tag{6}$$

$$R_{output} = 1/g_{m3} \tag{7}$$

$$A = g_{m2}/g_{m3} = 1 + R_f / R_s \tag{8}$$

With R_f defined by the wanted LNA gain and transistor sizing by the respective transconductances. It is important to note that noise canceling can occur only for the matching stage M_{1a}-M_{1b}. Noise generated by R_f and the noise canceling stage M_{2a}-M_{2b} will still appear at the output. This remaining noise, after cancellation of M_1 noise, gives the following noise factor expression:

$$F = 1 + \frac{R_s}{R_f} + \left(\frac{1}{R_s} + \frac{3}{R_f} + \frac{2R_s}{R_f^2} \right) \frac{ENF}{g_{m2}} \tag{9}$$
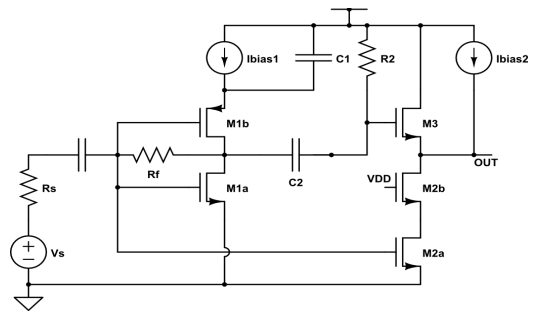

Figure 3 – Wideband noise canceling LNA.

Where the ENF (Excess Noise Factor) has value greater than 1 for submicron MOSFET. From Eq. 9, an increase of g_{m2} or R_f would lower NF, but changing these parameters could disrupt the noise canceling condition and make the noise from M_{1a}-M_{1b} reappears in the expression, increasing the noise factor. In [13], it is showed that in some conditions a partial noise canceling can be traded for a lower noise in the cascode stage, given indeed a lower overall noise factor.

The required noise figure for an HBC receiver following the IEEE 802.15.6 standard is 10dB [15], considering that the remaining blocks in the receiver chain will also add some noise, and that this noise is attenuated by the LNA gain we specify a gain of 10 and a noise figure of about 3dB over the frequency range of 1-100MHz.

HBC receivers do not require 50Ω input matching, since they use metal electrodes, instead of antennas, to couple the signal to the body [1]. The skin-electrode impedance is around hundreds of Ohms for frequencies in the MHz range, so we set the source resistance to 400 Ω based in [2]. Designing the LNA with higher input impedance will allow for both better impedance matching with the electrodes and for lower current consumption in the inverter stage, given the lower g_m required. At the output, matching to 50 Ω is not necessarily an issue for consumption since M_2 noise reduction will be the main aspect leading to high current consumption, so we kept 50 Ω as load impedance.

Given the design considerations made above and taking Eq. 6 to Eq. 8 we found: $g_{m1a} = g_{m1b} = 2.5$mS, $g_{m3} = 20$mS, $g_{m2} = 220$mS and $R_f = 4$ kΩ. The filter R2 = 95 kΩ and C2 = 10pF were set to allow proper coupling of the signal above 1MHz, and C_1 =14pF was chosen to enable AC grounding of M_{1b}. The final value for these components were further tweaked to reach the desired frequency band, and to consider trade-offs between noise canceling, power consumption and performance: g_{m2} and g_{m3} were lowered to values that simultaneously allowed lower power consumption and acceptable output matching; R_f was increased to improve noise canceling. Table 1 presents the final components values.

Table 1 – Components values

Component	Value
M1a (m/m)	17.6u/180n
M1b(m/m)	17.6u/180n
R_f (Ω)	6.3k
C1(F)	14p
C2 (F)	10p
R2 (Ω)	95k
M3(m/m)	15u/180n
M2a(m/m)	1000u/180n
M2b(m/m)	350u/180n

IV. SIMULATIONS

At first, a simulation was performed to verify the noise canceling principle: Figure 4 presents the noise figure results for the full circuit connected as in Figure 3, and for the connection between the inverter (M_{1a}-M_{1b}) output and M_3 input open, so that the noise from the inverter could not be added and canceled through M_3. As can be seen, the noise figure was higher when M_3 was open.

The noise figure results obtained from simulations considering primary schematic and post-layout extracted circuit are presented in Figure 5. The circuit layout appears in Figure 6, with a total area of 200um x 160um. Operation at the lower MHz frequency band limited the effects of layout parasitics and kept the performance very close to each other. Simulations results for Monte Carlo runs and process corners were performed over the range of 1-100MHz to verify consumption, S-parameters and noise figure. The relevant results are presented in Table 2.
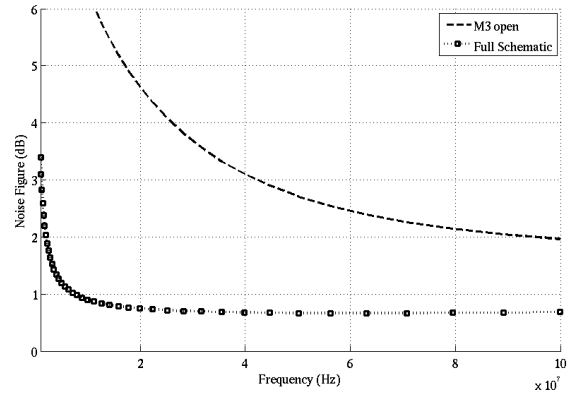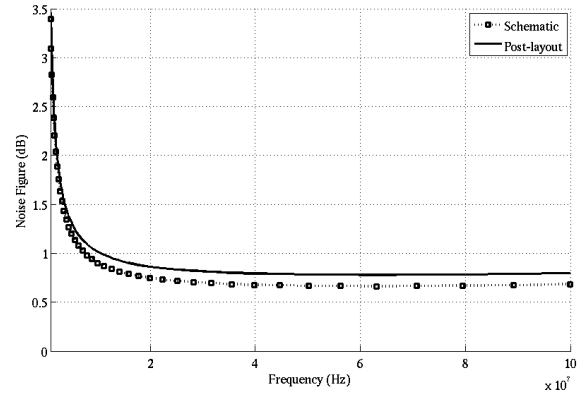

Figure 4 – Noise canceling test.

Figure 5 – Simulated noise figure for schematic and post layout.

Overall, the results for S-parameters indicate to acceptable performances concerning gain and matching. Regarding noise, the difficulty to achieve the desired noise figure over the entire

band seems to be related to the R_2C_2 filter at M_3 input, that could be degrading the signal phase at low frequencies, harming the noise canceling, and rising the 1/f noise. However, if we limit the operation between 10-100MHz, the noise figure is always lower than 1.23 dB and the power consumption achieved agrees with most noise canceling designs presented in the literature using the same topology [13], [14], [16]. However, most of them operates at higher frequencies, avoiding the difficulties we encountered near the very low MHz band. In Table 3 it is presented the comparison between this work and other wideband LNA in the literature. For a proper evaluation we used Eq. 10 as FOM (Figure of Merit), where S_{21}(in absolute units) is the gain, BW (Hz) is the bandwidth, f_c (Hz) is the bandwidth center frequency, F (in absolute units) is the noise factor and P_{dc}(W) is the power consumption. This expression was modified from the definition presented by ITRS (International Technology Roadmap for Semiconductors) [17] to better capture the performance of wideband designs. The HBC designs of [10], [11] performed better (higher FOM) than our LNA, essentially because of the power consumption, however designs using the same circuit topology had comparable performance.

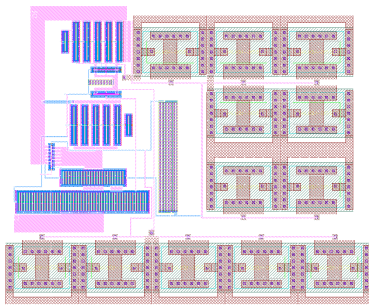$$FOM = \frac{S_{21} \cdot BW / f_c}{F \cdot P_{dc}} \qquad (10)$$

Figure 6 – LNA layout.

Table 2 – Corners and Monte Carlo (MC) Simulations results.

Corners	FF	FS	SF	SS	TT	MC Mean	MC Sigma
I_{dc} (mA)	11.09	10.49	9.70	9.26	10.07	10.03	0.42
NF (dB)	3.62	3.65	3.80	3.78	3.46	3.81	1.2
S_{11} (dB)	-8.74	-8.85	-9.88	10.05	-9.43	-9.43	0.80
S_{12} (dB)	-39.89	-39.27	-41.03	-40.49	-40.21	-40.22	1.20
S_{21} (dB)	17.60	17.85	13.84	14.17	15.75	15.58	1.88
S_{22} (dB)	-6.85	-7.38	-5.67	-6.03	-6.44	-6.46	0.88

Table 3 – Comparison with published HBC and the designed wideband LNA.

	This work[1]	This work[2]	[10]	[11][3]	[13]	[14]	[16]
P_{dc} (mW)	18	18	2.16	0.6	35	18	17.46
NF (dB)	3.81	1.23	3	3	2.4	4.9	3.99
S_{21} (dB)	15.58	15.58	16	13	13.7	12.1	16.42
BW(MHz)	100	90	40	80	1600	1460	1490
f_c(MHz)	50	55	50	80	800	730	755
FOM(mW^{-1})	0.28	0.42	2.10	3.73	0.16	0.14	0.3

[1]BW = 1-100MHz, [2]BW = 10-100MHz, [3]based on lowest NF

V. ACKNOWLEDGMENTS

VI. CONCLUSION

This paper presented the design of an inductorless wideband LNA for HBC, exploiting the noise canceling technique, designed in a CMOS 180nm/1.8V process. It operates between 1-100MHz, has a gain of 15.58 dB, noise figure of 3.81 dB, S_{11} of -9.43 dB and S_{22} of -6.46 dB. Even though performance metrics are within the application requirements, the power consumption to achieve low noise at low frequencies is the main drawback of this topology for BAN (Body Area Network) applications.

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