A 2.4 GHz Fully-Integrated CMOS Class-AB Power Amplifier

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***Abstract*—A Class-AB 2.4 GHz Power Amplifier (PA) is presented in this paper. The input stage is an input driver and the second stage is the power core. The components were integrated on the same chip in a 0.18-μm CMOS process. The simulation results show that the PA achieves high power gain of 23dB with output power of 12.45dBm and drain efficiency of 41%.**

***Index Terms*—CMOS, Class-AB, Power Amplifiers, Load Pull, Output Matching Network.**

I. Introduction

A Power Amplifier (PA) is a circuit designed for delivering high power signal to a load, while keeping the efficiency as high as possible. Trends in the design of these circuits include its full integration in CMOS technologies and adressing the trade-offs between supply voltage, output power, power efficiency and linearity [1].

Usually, PAs are implemented using off-chip components.In [2], the drain inductors are implemented by bonding wires and, therefore the value of inductance cannot be ascertained due to the uncontrollability of the length of the bonding wire and this aggravates the problems. However, a differential structure is needed to ensure that the parasitic inductance of bonding wire can not influence the performance of PA.

On the other hand in [3], the PA is implemented with all passive components including the drain inductors and output matching network integrated by on chip components, reducing the errors introduced to the output matching network. Although, using on chips components the transformation ratio of ouput matching network should not be too great due this degrades the efficiency and output power. The difficulties associated to the design of a fully integrated PA solution include the unavailability of high quality factor passive devices, specially inductors, which are sometimes mitigated by using the bondwires as a design device.

The PAs can be also classified according to their operation condition. In [3] and [4] the PA is biased at Class-AB operation, which are widely used in wireless transceiver design due to their inherently high efficiency (around 78% theoretically) and relatively high linearity.

In this paper, a fully-integrated PA with high-power gain, operating at 2.4GHz is developed by using a two stages topology. The proposed topology is presented in Section II with the design metodology and the simulation results considering the layout parasitics being shown in Sections III and IV respectively, and the conclusion in Section V.

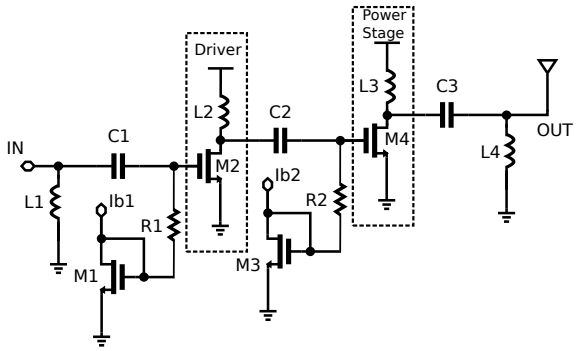

Fig. 1. Topology of proposed PA

II. Proposed Topology

The presented PA consists of dual stage amplifier including input and output matching networks, as shown in Fig. 1. The input matching network provides a 50 Ω matching at 2.4 GHz between the driver and the source. This matching is performed to facilitate future measurements since it is necessary to identify the amount of power delivered by the source. The output maching network is designed to provide the optimum impedance to the power stage in order to achieve the highest output power at the antenna.

A. Power Stage

The power stage is biased at class AB operation to deliver power to the load, combining sufficient power efficiency and linearity. As shown in the Fig. 1, the transistor is biased with a diode-connected transistor (M3) and a 50kΩ resistor (R2) to prevent the signal return through this path. At the power stage, an important factor is the output impedance which is presented to the transistor. This impedance is obtained through the well-known Load-Pull Characterization method [1].

1) Output matching: After determining the impedance which the load must be transformed to, the next step is to choose the output matching network. This operation was performed through a π array (represented in Fig. 1 for L3, C3 and L4). Many authors do not consider the drain inductor as part of matching network [1]. However at case where all components are integrated on the same chip, the inductance value of this drain inductor will not be large enough to be disregarded. Meanwhile, during the design of the π-network it is important to ensure that the parasitic shunt resistance

(R_p) effect of the inductor losses have to be the largest possible to minimize power losses. Then the inductor should be configured to achieve the highest possible quality factor (Q). Equation (1) shows an approximation between Q, R_p and the inductance value (L).

$$R_p = \omega_0 L Q \tag{1}$$

Above in the equation number (1), it can be seen that Q and L are correlated. Then for bigger R_p, the inductance value (L) must be varied directly proportional with a high quality factor.

B. Driver Stage

The Driver stage is biased at class A operation to ensure linearity. This stage is used to deliver a sufficiently amount of power for the power stage and to drive the large input capacitance of this stage. Another important detail of this stage is the input matching network which must provide a 50Ω input matching impedance with the source.

1) Input matching: The input matching is a L-matching network,which is composed by two passive elements ($L1$ and $C1$) as seen in Fig.1. For good matching in high frequencies, $S_{11} \leq -15$dB should be maintained.

III. Design Methodology

As previously mentioned in the design of power stage an important factor is the output impedance which is presented to the transistor. In [3] this impedance is found by a technique called load-line match method. In this paper the methodology is the load-pull measurement. With respect to design metodology is important also explain as is ensured the stablity of PA and the metric used to define the efficiency.

A. Load-Pull

The Load-Pull Characterization is performed by measuring the amount of mismatch which may exist between the amplifier and the load to deliver the highest power. For this purpose the magnitude and phase of reflection coefficient between amplifier and the load are swept by simulation. Hence, the optimum impedance for the load is obtained from power contours plots on the Smith chart [1], as shown in Fig. 2. The power contour which correspond to the maximum output power is the innermost countour seen in the figure.

B. Stability

The stability of the Power Amplifier is guaranteed by choosing the impedance presented to the amplifier by both the input and output matching networks. Thus, when the optimum output impedance is chosen based on the load pull characterization, the stability circles of the load and the source should be taken into account [5]. Since the input impedance is fixed for the condition of 50Ω input matching, the stability of the power amplifier must be attended only by means of the load impedance. After the load impedance has been chosen based on stability circles, the simulation of K and B_{1f} must be made to check the stability condition [6]. K is the stability factor, and the B_{1f} is the alternative stability factor, given by, respectively, equations (2) and (3).

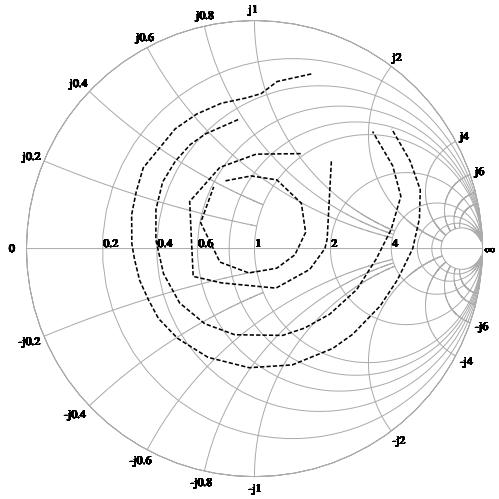

Fig. 2. Load Pull Contours exemple for 2.4 GHz

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2}$$

$$B_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{3}$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{4}$$

Both of them are considered in the stability analysis performed by the simulator. In order to have an unconditionally stable amplifier this analysis must result in $K > 1$ and $B_{1f} > 0$.

C. Drain Efficiency

Some research works presented the efficiency of PA as Power added afficiency [3], [4].In this work the metric used is the drain efficiency, which is represented by equation (5).

$$Drain\ Efficiency = \frac{P_{load}}{P_{DC}} \tag{5}$$

In the equation above P_{load} represents the output power in the load, and P_{DC} is the DC consumption of PA. In this paper the Drain Efficiency results and Consumption are refers to the Power stage.

IV. Simulation Results

The proposed class-AB PA with input driver was fully integrated and implemented in a 0.18-µm CMOS technology. It was simulated at 2.4 GHz with 2 V of power supply in both driver and power stage. The layout of circuit is depicted in Fig. 3. The die size is 1500 x 1500 μm^2. The driver and power stage consist of 30 and 25 set of transistors respectively with $W/L = 20\mu m/0.4\mu m$ each. Figure 4 presents the 1 dB compression point of the PA. This analysis was performed by doing a sweep on power input. In the Fig. 4 is observed Pin x Pout and that the 1 dB compression point is -11.83 dBm. This result shows that PA is not operating well above the 1

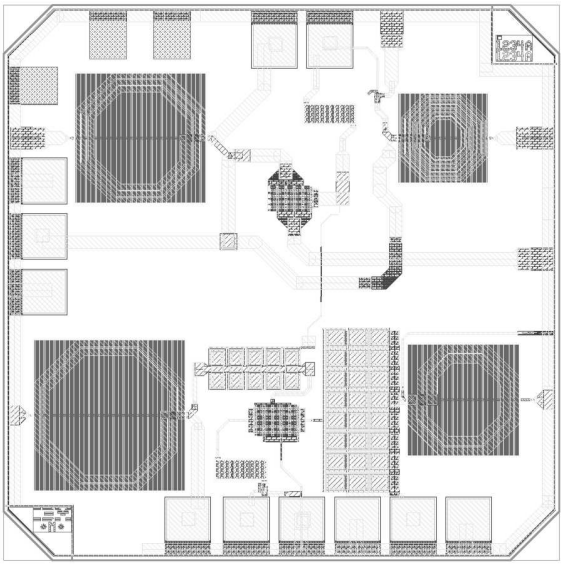

Fig. 3. Layout of Power Amplifier

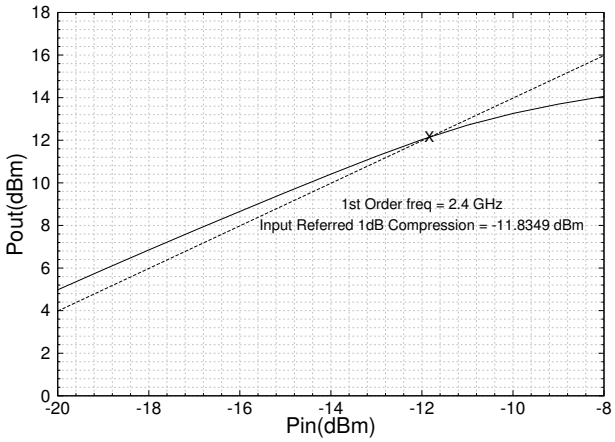

Fig. 4. Curve of 1dB Compression Point

dB compression point since the input power is -11.42, thus it is not operating in a region in which distorts more. The PA delivers a saturated power P_{sat} of 15 dBm. Figure 5 presents the Output Power of PA. At 2.4GHz the PA presented an Ouput Power of 17.57 mW and in the second and third harmonic, 71.17 μW and 12.46 μW respectively. With the analysis of Output Power is possible to observe that the PA not amplify in the second an third harmonic. This means that the PA is well centered on the frequency of operation.

The PA's stability was also analyzed.This analysis was performed for a frequency range of 2 GHz to 25 GHz, Fig. 6 and Fig. 7 present the results of this analysis proving that PA is unconditionally stable.

S_{11} was also extracted from the S-parameters simulation in order to check the condition of 50Ω input match. In Fig. 8 is presented the S_{11}=-20.38 dB and the bandwith of this matching of 112 MHz. This results prove that there is a good matching between the driver and the source at high frequencies.

The process variation effects were estimated by Corners and

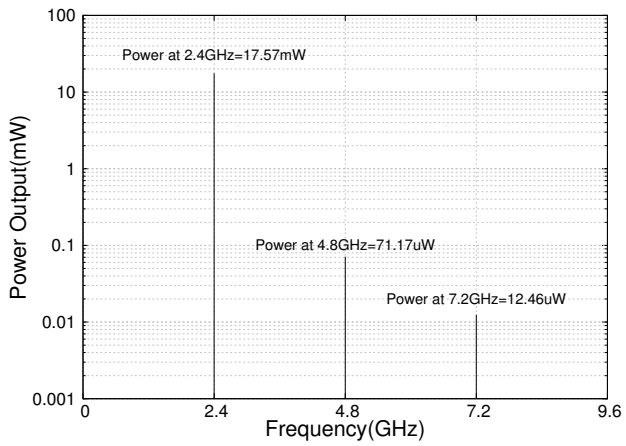

Fig. 5. Spectrum of Output Power

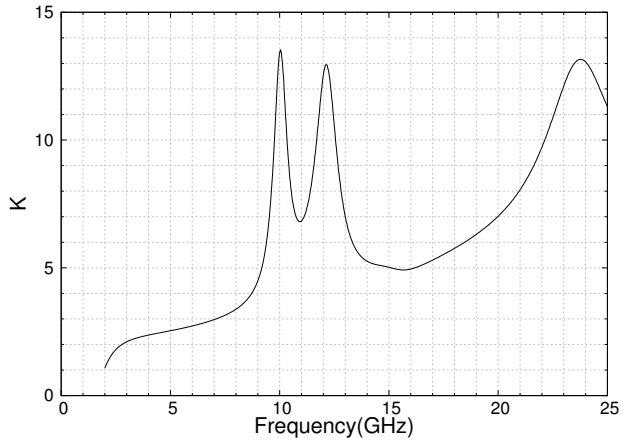

Fig. 6. Stability factor K

MonteCarlo simulations considering the following figures of merit: the drain efficiency and power consumption, referred to the power stage, and output power, S_{11} and the stabilities parameters. In the corners analysis was perfomed only the corners cases ff, ss, fff and ssf due the PA has only NMOS transistors. The MonteaCarlo analysis was perfomed with 442 samples.Table I summarizes the Corners results and Table II illustrates the MonteCarlo Analysis, where σ is the standard deviation, μ is the mean value and N is the number of samples.

TABLE II
MONTECARLO ANALYSIS

	σ	μ	N
Output Power	1.7376mW	17.35mW	442
Power Consumption	1.6494mW	41.924mW	442
K	0.032	1.7087	442
B_{1f}	0.004	0.857	442
S_{11}	1.034dB	-20.2789dB	442
Efficiency	2.67%	41.4%	442

V. CONCLUSION

A fully-integrated 2.4 GHz power amplifier implemented in standard CMOS 0.18-μm technology was presented. By using

TABLE I
CORNERS ANALYSIS

Corner	Output Power (mW)	Power Consumption (mW)	K	B_{1f}	S_{11} (dB)	Efficiency (%)
Nominal	17.57	42.08	1.7	0.856	−20.38	41.75
ff	21.64	46.02	1.652	0.856	−22.09	47.02
ss	13	37.53	1.765	0.855	−18.75	34.63
fff	23.03	47.4	1.638	0.855	−22.8	48.58
ssf	12.03	36.57	1.779	0.855	−18.42	32.89

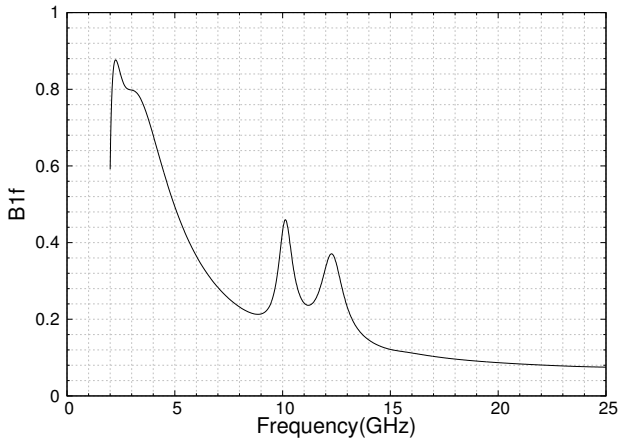

Fig. 7. Alternative stability factor B_{1f}

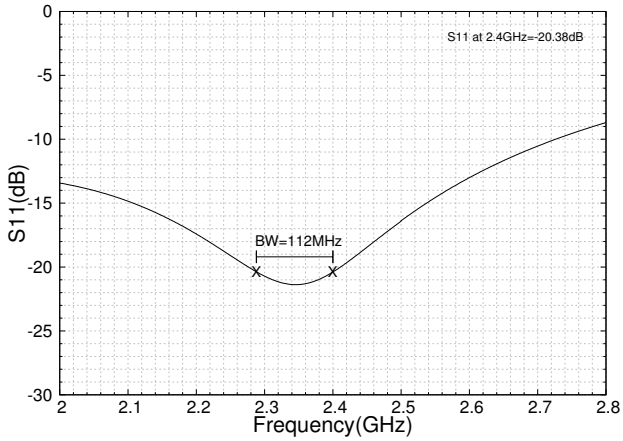

Fig. 8. Curve of S-parameters analysis for S_{11}

a driver and power stage as well as on-chip input and output-matching networks the presented PA achieves high gain and high output power. It can submit an output power of 12.45 dBm with 41% of drain efficiency, in the power stage, for a input power of -11.42 dBm. The corners and montecarlo analysis showed good accuracy with the typical simulations.

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