A 2.4GHz Cascode CMOS Low Noise Amplifier

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Summary

1. Introduction
2. Design Methodology
3. Simulation and Measurement Results
4. Conclusion

Summary

1 Introduction

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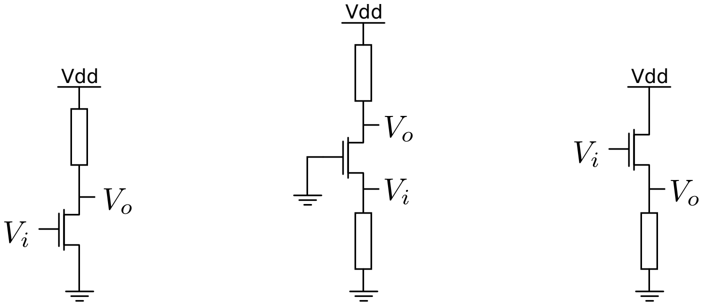
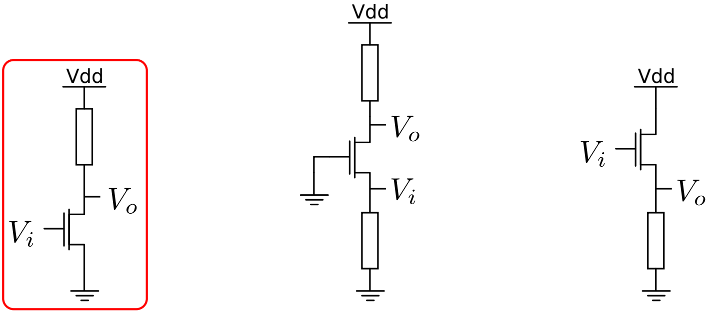
Goal

- Applications require low power and small footprint
- The goal of this work is to design a low noise amplifier for:
  - ISM 2.4GHz
  - $50\,\Omega$ input and output impedances
  - $0.18\,\mu\mathrm{m}$ CMOS technology
  - $1.8\,\mathrm{V}$ supply voltage

Single transistor amplifiers



- LNAs are usually designed with a single transistor:
  - Common-source: Driver; Poor reverse isolation
  - Common-gate: Matching with higher bandwidth; Noise
  - Common-drain: gain $\approx$ 1; buffer



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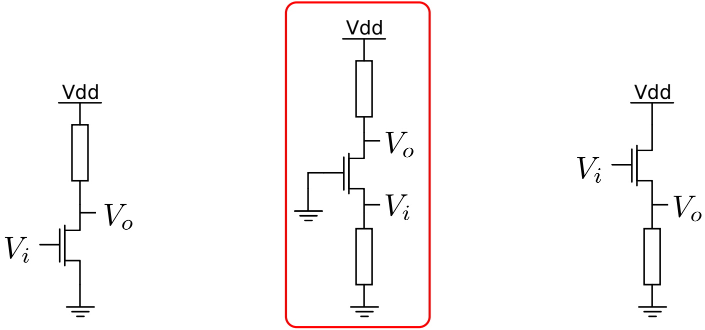

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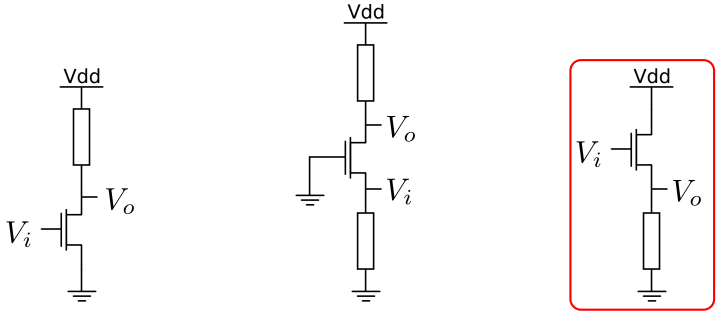

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Cascode amplifier

- It is possible to obtain better results using combinations of the single-transistor topologies
- The cascode topology was chosen
  - Can maintain gain up to high frequencies
  - High reverse isolation
  - Reduces voltage swing at the output
  - Cannot be as low-noise as a single transistor amplifier due to the noise added by the second element

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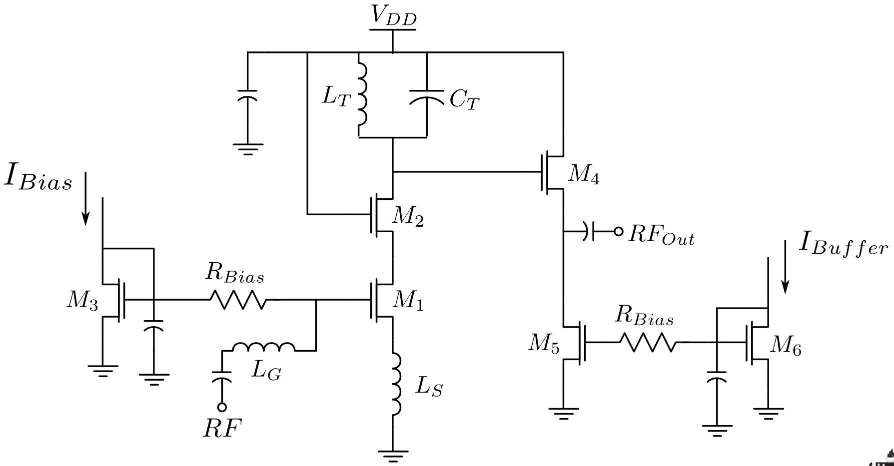

V_{DD}
L_T
C_T
I_{Bias}
M_4
M_2
RF_{Out}
I_{Buffer}
R_{Bias}
M_3
M_1
R_{Bias}
M_5
M_6
L_G
L_S
RF

Design Methodology

- STEP 1: Current density that provides the lowest NF_{min}

$$v_{no,r_g}^2 \approx 4kTr_g g_{m1}^2 R_L^2 \propto I_D$$
$$v_{no,i_d}^2 \approx 4kT\gamma g_{m1} R_L^2 \propto \sqrt{I_D}$$
$$v_{no,i_g}^2 \approx \frac{4}{5} kT\delta\omega^2 C_{gs1}^2 g_{m1} R_L^2 \propto \sqrt{I_D}$$
$$P_{out} = \frac{v_{out}^2}{R_L} = g_m^2 v_{in}^2 R_L \propto I_D$$

- Increasing I_D should decrease NF, but at higher currents other effects are observed.
- Lowest NF_{min} at $I_D/W = 60\,\mu\mathrm{A}/\mu\mathrm{m}$

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Design Methodology

- STEP 2: Size the transistor making $\Re\{Y_{opt}\} = 1/50$ S

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2$$

  - L of transistors is kept minimum for maximum f_T
  - W $= 46.5\,\mu\mathrm{m}$

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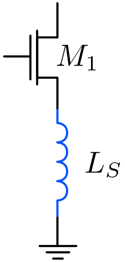
- STEP 3: place and size L_S for $\Re\{Z_{in}\} = 50\,\Omega$.

$$Z_{in}(s) = \frac{1}{sC_{gs1}} + s(L_S + L_G) + \frac{g_{m1}}{C_{gs1}} L_S$$

  - $L_S = 1.55nH$

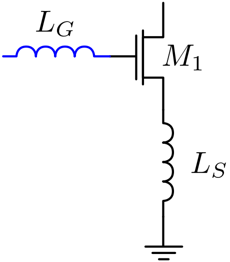


Design Methodology

- STEP 4: Place and size the L_G so that $Im\{Z_{in}\} = 0$

$$L_G = \frac{1}{\omega^2 C_{gs1}} - L_S$$

  - $L_g = 20.27nH$



- The W of cascoded transistor (common-gate) was chosen to provide enough gain and low parasitic capacitances
- The W of the buffer transistors were chosen to present low parasitic capacitances and provide $50\,\Omega$ output impedance at a reasonable I_{Buffer}
- The tank circuit was designed to resonate at 2.4GHz, parasitic capacitances must be considered

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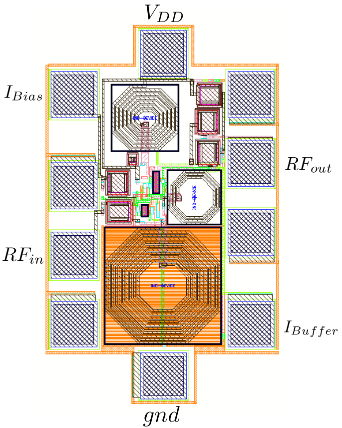
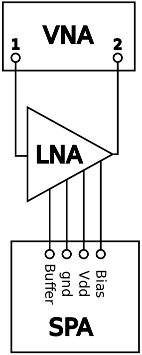
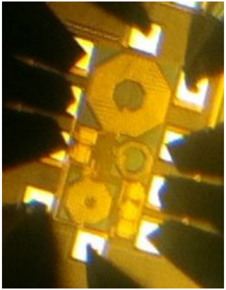
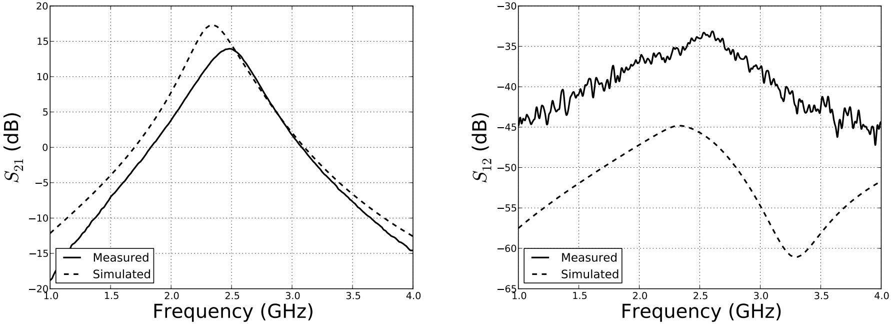
Layout and Test-bench







S-parameters Measurement and Comparison



- At 2.4 GHz
  - $S_{21,meas} - S_{21,sim} = 14.5 - 16.8 = -2.3$ dB
  - $S_{12,meas} - S_{12,sim} = -34 - (-45) = 11$ dB

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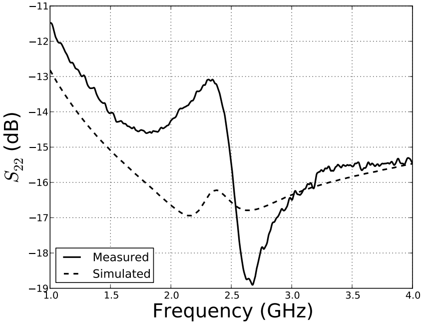
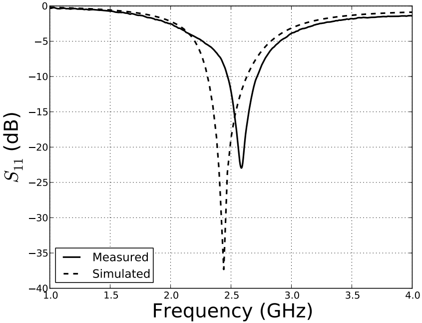
S-parameters Measurement and Comparison





- At 2.4 GHz
  - $S_{22,meas} - S_{22,sim} = -13.1 - (-16.2) = 3.1$ dB
  - $S_{11,meas} - S_{11,sim} = -8 - (-23) = 15$ dB

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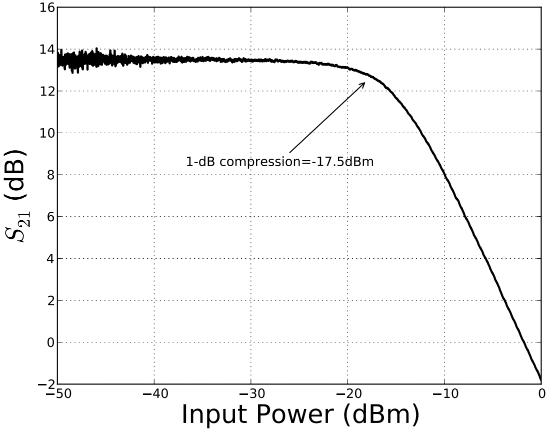
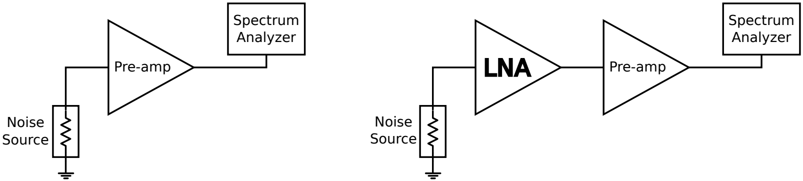
Linearity analysis



- IIP3 = -7.8 dBm
- Simulation IIP3 = -6.6 dBm

Measuring Noise Figure (Y-Factor Method)

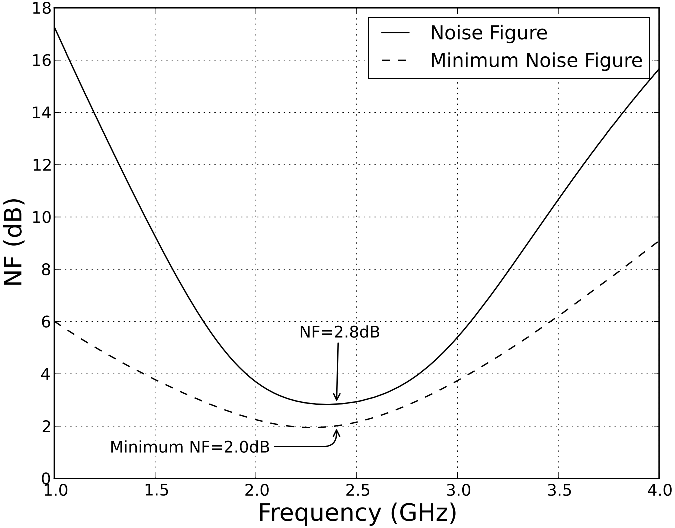


$$ENR = \frac{T_H - T_C}{T_0}$$

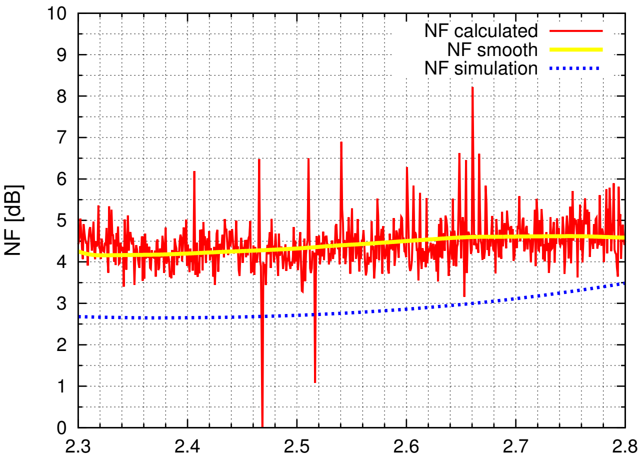
$$F_T = \frac{ENR}{Y - 1}, \text{ where } Y = \frac{N_{off}}{N_{on}}$$

$$F_{LNA} = F_T - \frac{F_2 - 1}{G_{LNA}}$$

Noise Figure in post-layout simulation



Noise Figure



- NF = 4.2 dB at 2.4 GHz (2.8 dB in simulation)

Comparison with recent works

Parameter	[1]	[2]	[3]	[4]	[5]	This Work
Gain (dB)	20	15	4.5	14.6	23	14.5
NF (dB)	4	3.6	2.77	3.8	3.8	**4.2**
IIP3 (dBm)	-12	-14.3	11.8	-12	-9.1	-7.8
Core power (mW)	1.32	0.8	18	0.12	13	**5**
Area (mm^2)	0.007	-	0.55	-	4.1	**0.15**
Supply voltage (V)	1.2	0.8	1.8	0.6	1.0	1.8
Technology (nm)	130	130	180	130	180	180

1 F. Belmas, F. Hameau, and J. Fournier. A 1.3mW 20dB gain low power inductorless LNA with 4dB noise figure for 2.45GHz ISM band. In Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE, pages 1-4, june 2011.

2 S. Manjula and D. Selvathi. Design of micro power CMOS LNA for healthcare applications. In Devices, Circuits and Systems (ICDCS), 2012 International Conference on, pages 153 –156, march 2012.

3 Y. Shen, H. Yang, and R. Luo. A fully integrated 0.18μm CMOS low noise amplifier for 2.4-GHz applications. In ASIC, 2005. ASICON 2005. 6th International Conference On, volume 2, pages 582-586, oct. 2005.

4 T. Taris, A. Mabrouki, H. Kraimia, Y. Deval, and J.B. Begueret. Reconfigurable ultra low power LNA for 2.4GHz wireless sensor networks. In Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on, pages 74 –77, dec. 2010.

5 L. Zhenying, S. Rustagi, M. Li, and Y. Lian. A 1V, 2.4GHz fully integrated LNA using 0.18μm CMOS technology. In ASIC, 2003. Proceedings. 5th International Conference on, volume 2, pages 1062-1065 Vol.2, oct. 2003.

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Conclusion

- A Cascode CMOS LNA operating at 2.4 GHz with 4.2 dB NF and 14 dB gain was designed.
- The LNA was fabricated and tested.
- The S-parameters, linearity and NF were analyzed.
- It has been observed a shift in frequency in S_{11}, which was due to the inaccuracy in high frequency of the component models and process variation.
- The other S-parameters and linearity remained within specifications.
- The measured NF was 1.4 dB above the simulated.
- The LNA has a small area ($0.15\,\mathrm{mm}^2$).

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Thank you