A 25-dBm 1-GHz Power Amplifier Integrated in CMOS 180nm for Wireless Power Transferring

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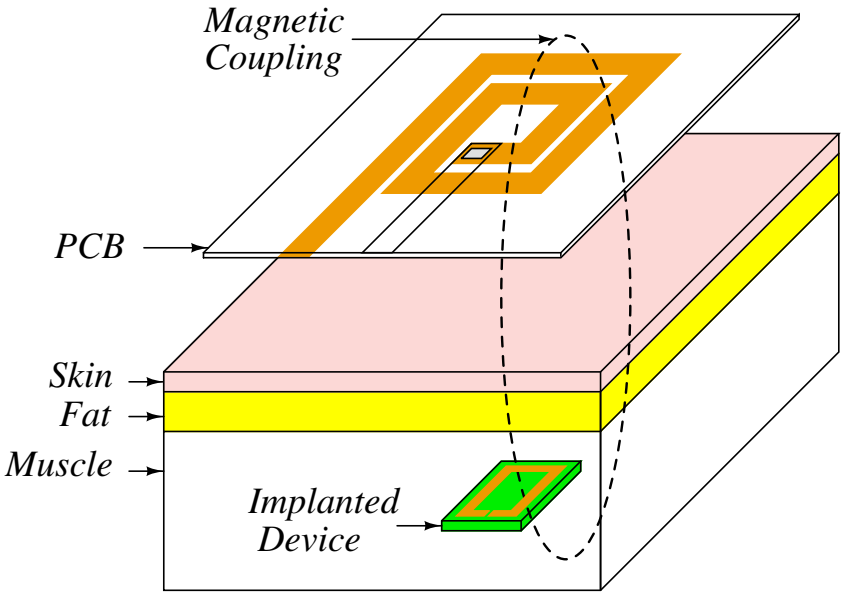
SBCCI 2015

Target application

- Implanted devices can significantly improves human health care.



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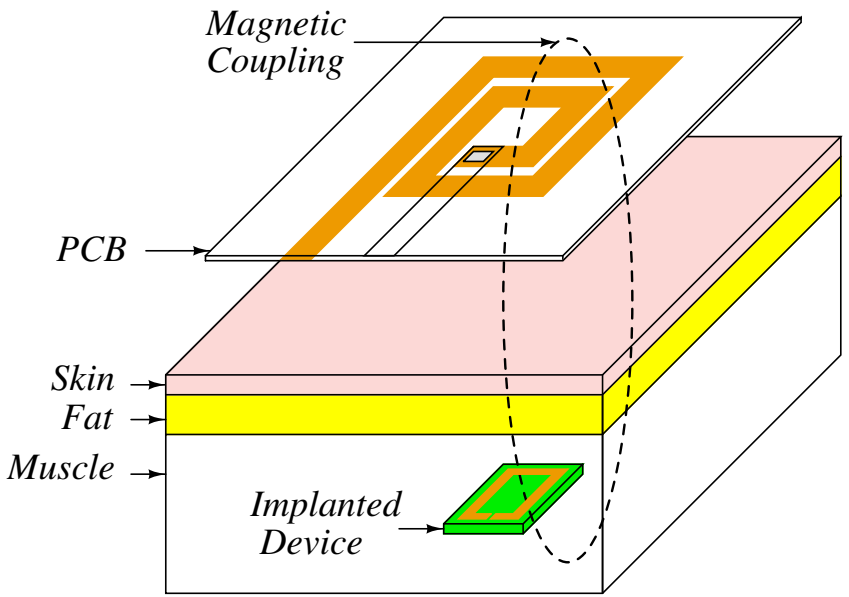
- Those devices need to be miniaturized and wirelessly powered.



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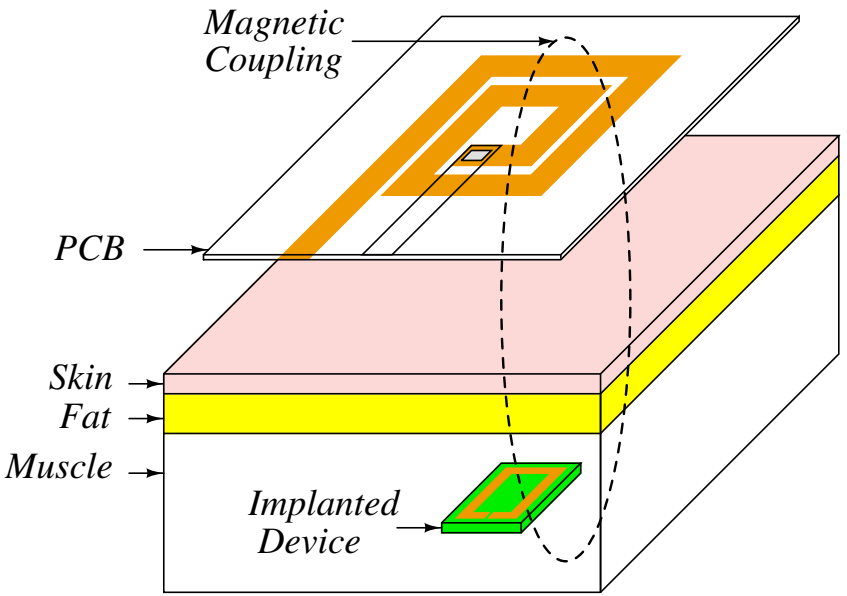

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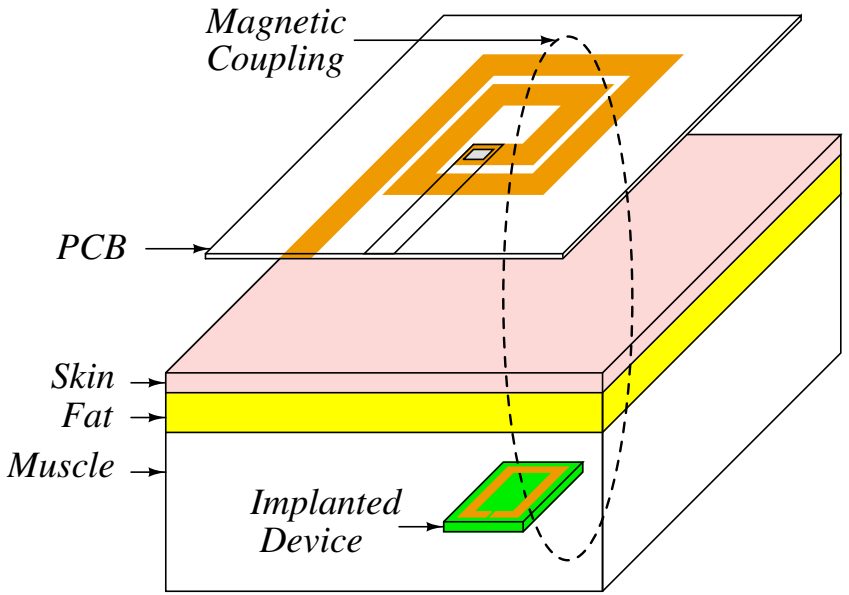
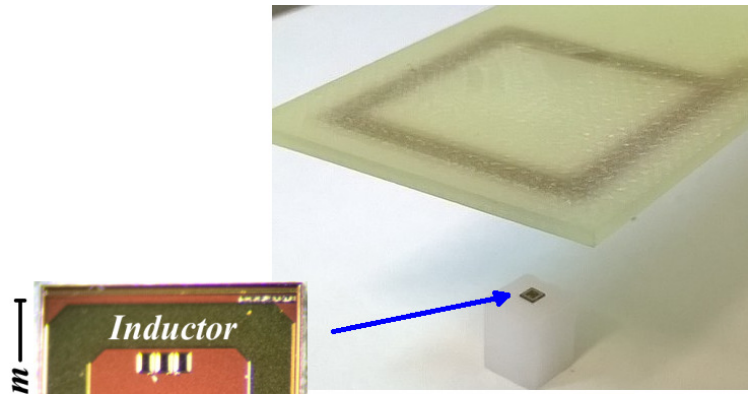
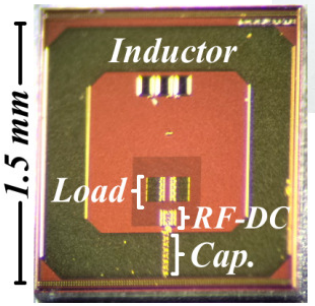




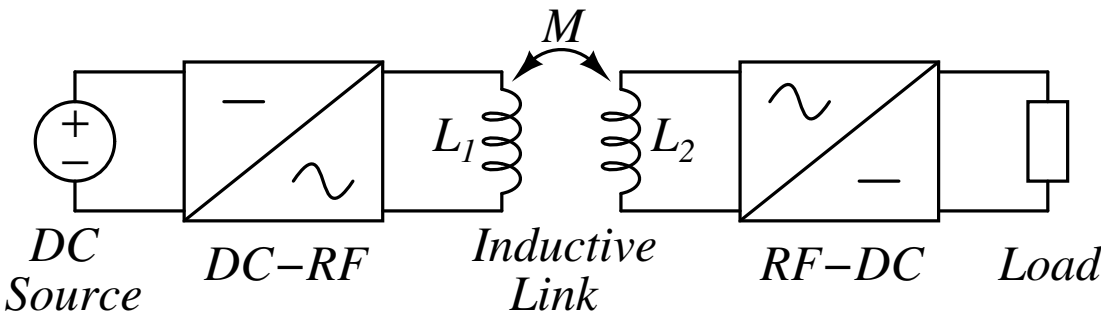


Frequency: 990 MHz

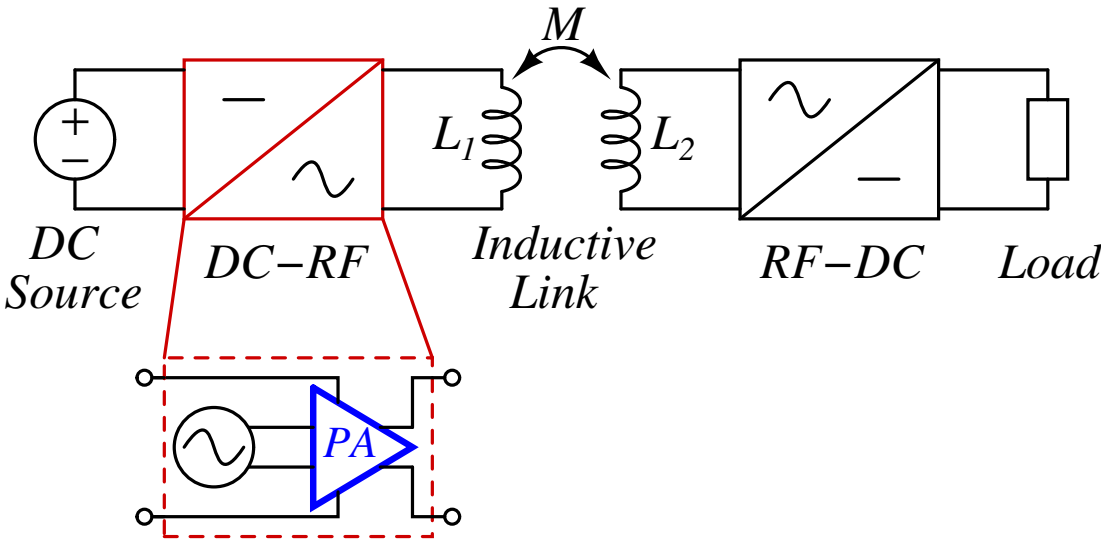
Power (primary): 25 dBm

[9] Fabian L. Cabrera and F. Rangel de Sousa, "A CMOS Fully-Integrated Wireless Power Receiver for Autonomous Implanted Devices," in *ISCAS* 2014.

Power amplifier



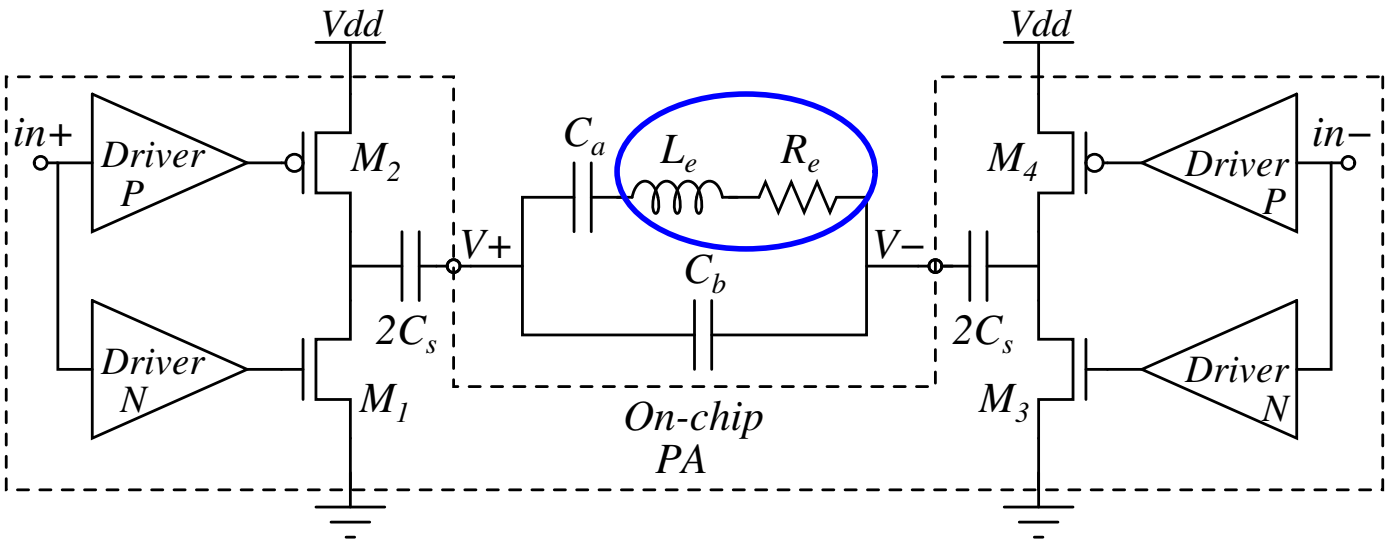
Power amplifier



Specifications:

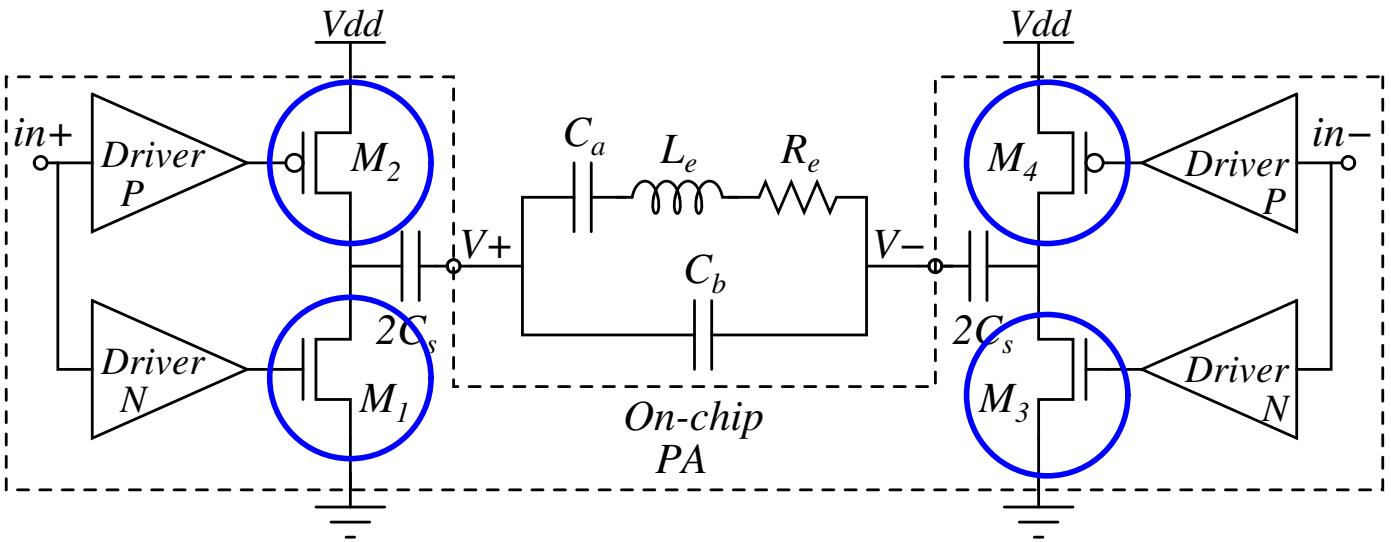
Frequency	990 MHz
Power	25 dBm
PA load	1.8+j57.8
Efficiency	Maximize
Integration level	Minimize number of external components
Configurability	Power level can be adjusted

Differential Class-D topology:



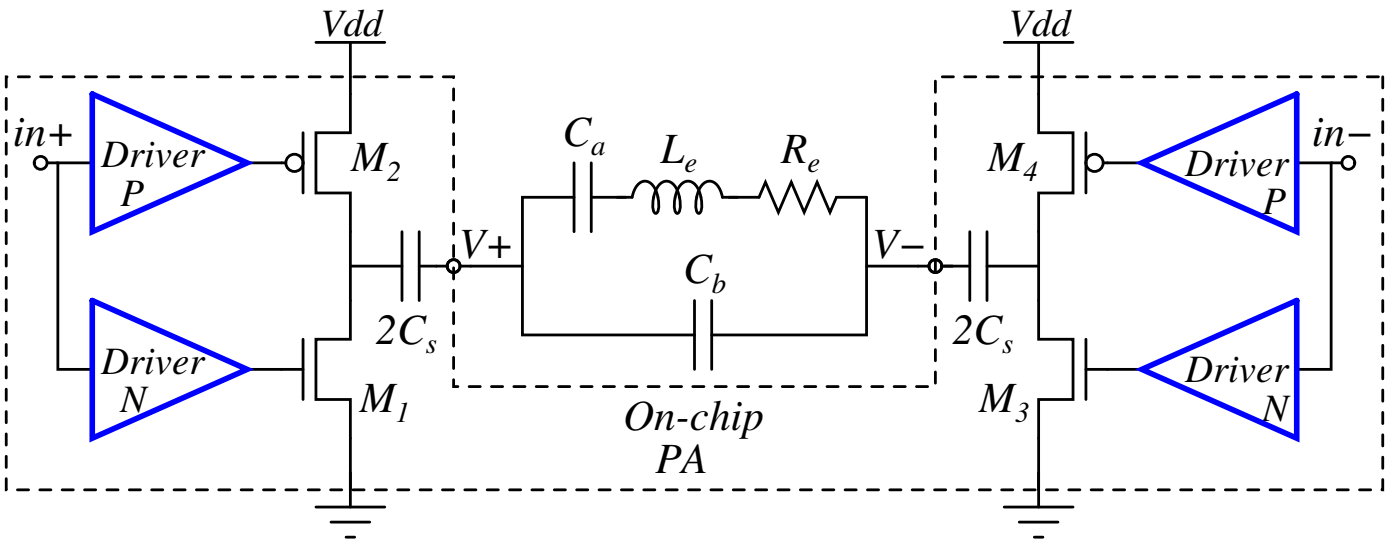
Equivalent Load

Differential Class-D topology:



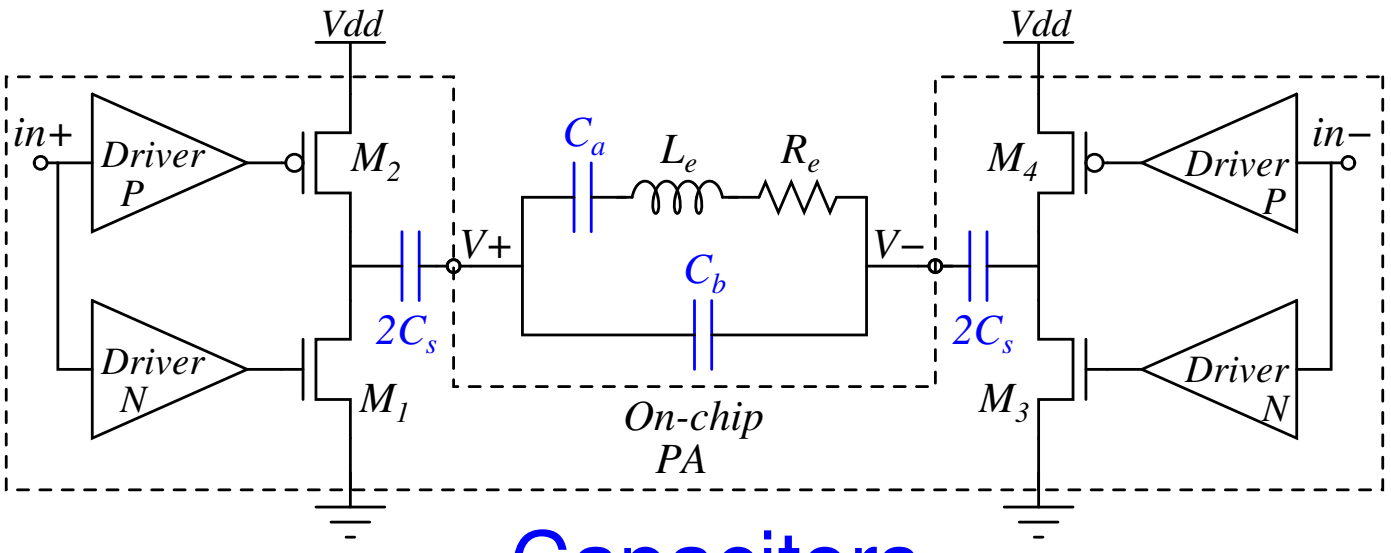
MOS switches

Differential Class-D topology:



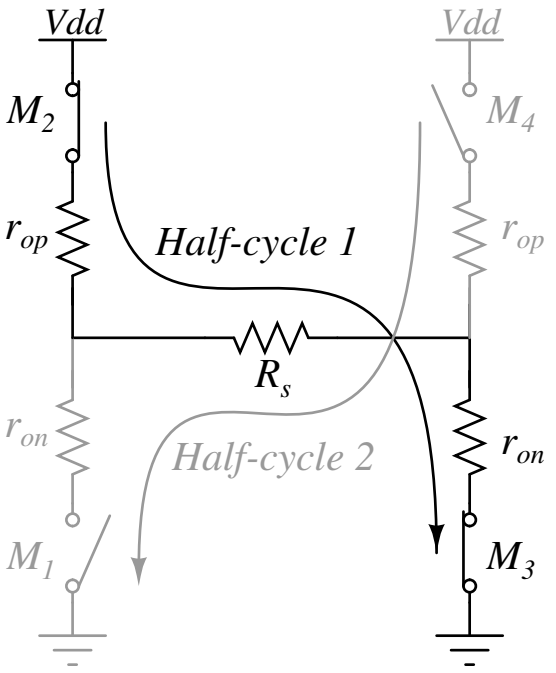
Drivers

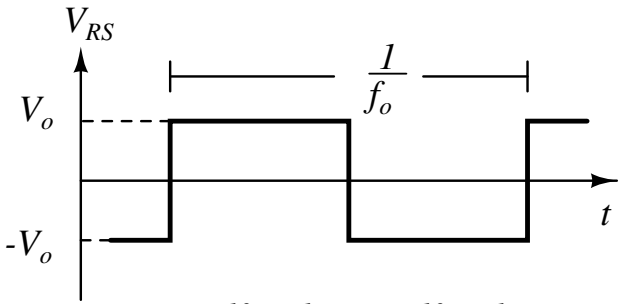
Differential Class-D topology:



Capacitors

- Impedance transformation
- V+ and V- voltage between +/- 5V


Vdd
Vdd
M2
M4
rop
rop
Half-cycle 1
Rs
ron
ron
Half-cycle 2
M1
M3


VRS
1
fo
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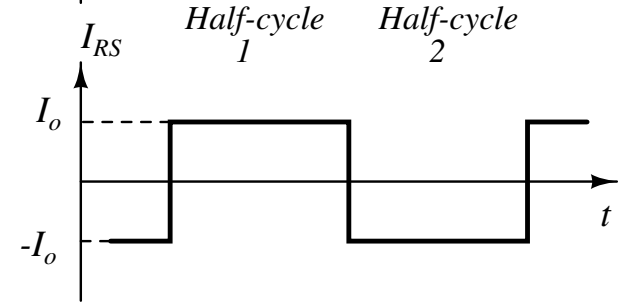
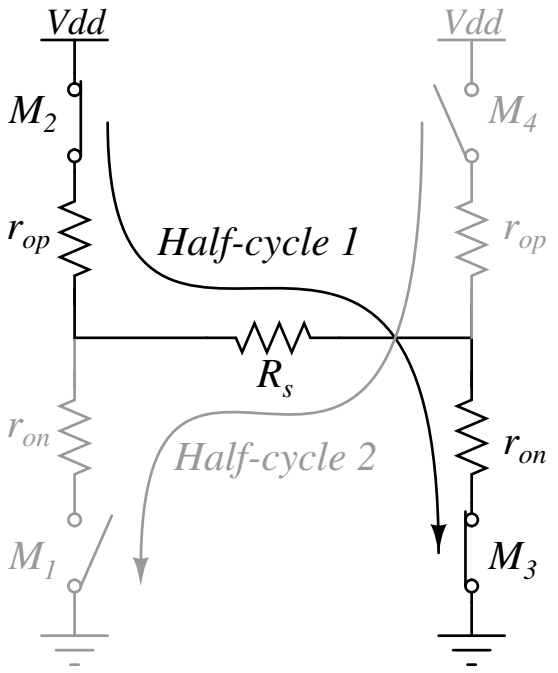
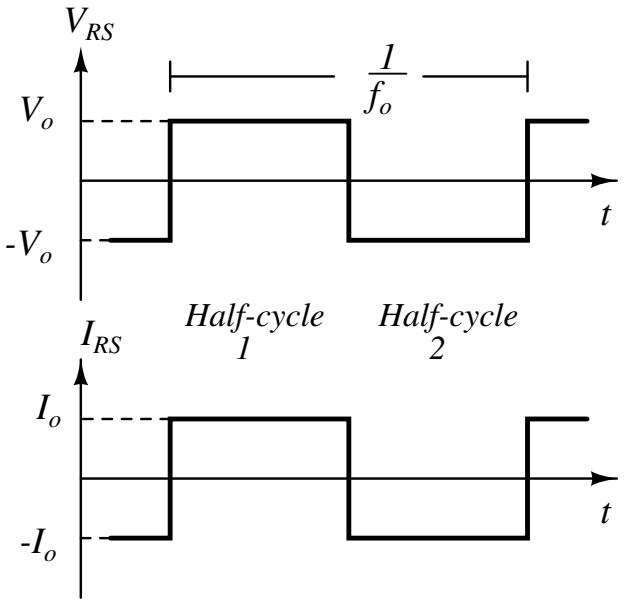

Half-cycle 1
Half-cycle 2
IRS
Io
-Io
t

Model





DC power delivered by V_{dd}:

$$P_{DC} = V_{dd} I_o = \frac{V_{dd}^2}{R_s + r_{on} + r_{op}}$$

Output power (fundamental frequency):

$$P_{Rs(1)} = \frac{1}{2}\left(\frac{4V_o}{\pi}\right)\left(\frac{4I_o}{\pi}\right) = \frac{8V_{dd}^2 R_s}{\pi^2 (R_s + r_{on} + r_{op})^2}$$

Power used to drive the switches:

$$P_{drive} = C_g V_{dd}^2 f_o$$

Efficiency

$$\eta = \frac{P_{Rs(1)}}{P_{DC} + P_{drive}} = \frac{1}{\frac{\pi^2}{8} + \frac{\pi^2 (r_{on} + r_{op})}{8R_s} + \frac{C_g V_{dd}^2 f_o}{P_{Rs(1)}}}$$

Sizing the transistors

$$r_{on} + r_{op} = \frac{a}{W} \qquad C_g = bW$$

Function to be optimized

$$\frac{1}{\eta} = \frac{\pi^2}{8} + \frac{\pi^2}{8} \frac{1}{\left(\frac{8V_{dd}^2 W}{\pi^2 a P_{Rs(1)}} - 2 \right)} + \frac{bWV_{dd}^2 f_o}{P_{Rs(1)}}$$

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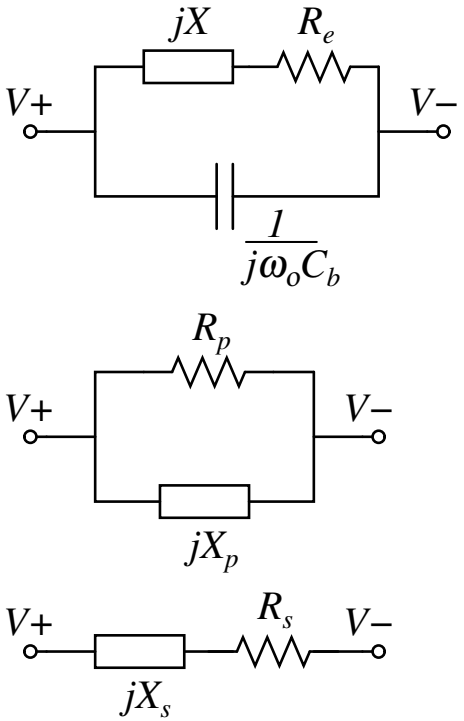
$$W_{opt} = \frac{\pi^2 a P_{Rs(1)}}{8V_{dd}^2} \left(\frac{1}{\sqrt{abf_o}} + 2 \right)$$

$$R_{sopt} = \frac{8V_{dd}^2}{\pi^2 P_{Rs(1)}} \left(\frac{1}{1 + 2\sqrt{abf_o}} \right)$$

$$\frac{1}{\eta_{max}} = \frac{\pi^2}{8} \left(1 + 2\sqrt{abf_o} + 2abf_o \right)$$

Impedance transformation network



$$R_p = \frac{V_H^2}{2P_{Rs(1)}}$$

$$C_a = \frac{1}{\omega_o\left(\omega_o L_e - \sqrt{R_e(R_p - R_e)}\right)}$$

$$C_b = \frac{1}{\omega_o R_p}\left(\sqrt{\frac{R_p}{R_e} - 1} - \sqrt{\frac{R_p}{R_s} - 1}\right)$$

$$C_s = \frac{1}{\omega_o\sqrt{R_s(R_p - R_s)}}$$

Design Methodology

1	$P_{Rs(1)}$	316	mW	4	a	4.3	mΩ.m
	f_o	990	MHz	5	W_{opt}	3.9	mm
	R_e	1.8	Ω		R_{sopt}	6.1	Ω
	L_e	9.3	nH	6	$\lvert V_{dsp}\rvert$	220	mV
	V_{dd}	1.8	V		V_{dsn}	54	mV
	V_H	9	V	7	C_s	5.9	pF
2	R_p	128.1	Ω		C_a	3.8	pF
3	b	7.8	nF/m		C_b	4.9	pF

1. Define the specifications and constraints.

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2. Calculate the value of R_p:

$$R_p = \frac{V_H^2}{2P_{Rs(1)}}.$$

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3. Obtain from simulation the PMOS and NMOS gate capacitance parameter.

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2	R_p	128.1	Ω		C_a	3.8	pF
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4. Also obtain the PMOS and NMOS equivalent resistance parameter, assuming an initial value for $V_{dsp,n}$.

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2	R_p	128.1	Ω		C_a	3.8	pF
3	b	7.8	nF/m		C_b	4.9	pF

5. Calculate optimal values for W and R_s:

$$W_{opt} = \frac{\pi^2 a P_{Rs(1)}}{8V_{dd}^2}\left(\frac{1}{\sqrt{abf_o}} + 2\right)$$

$$R_{sopt} = \frac{8V_{dd}^2}{\pi^2 P_{Rs(1)}}\left(\frac{1}{1 + 2\sqrt{abf_o}}\right)$$

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2	R_p	128.1	Ω		C_a	3.8	pF
3	b	7.8	nF/m		C_b	4.9	pF

6. Find $|V_{dsp}| = I_o r_{op}$ and $V_{dsn} = I_o r_{on}$.

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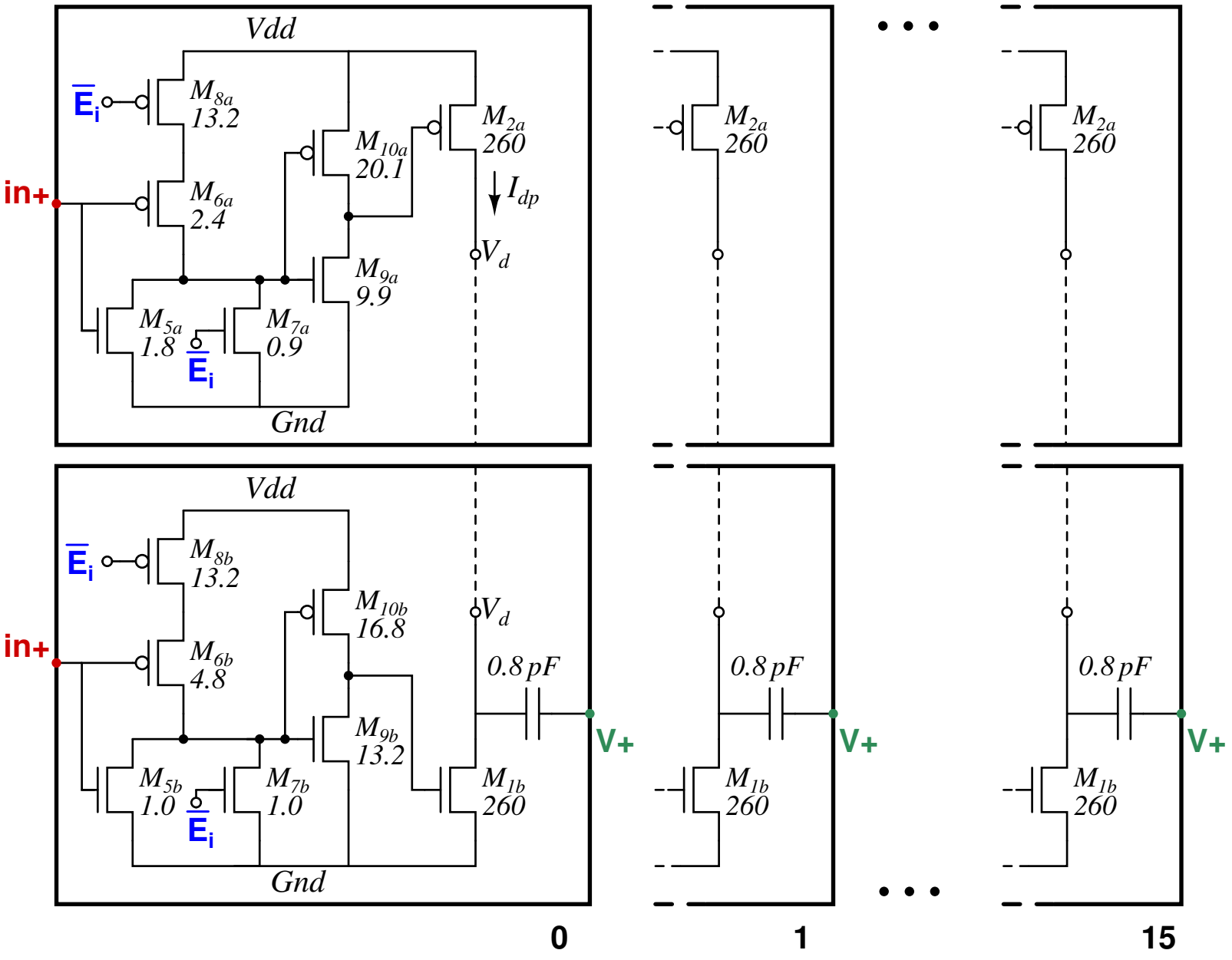
7. Calculate the capacitances C_a, C_b and C_s:

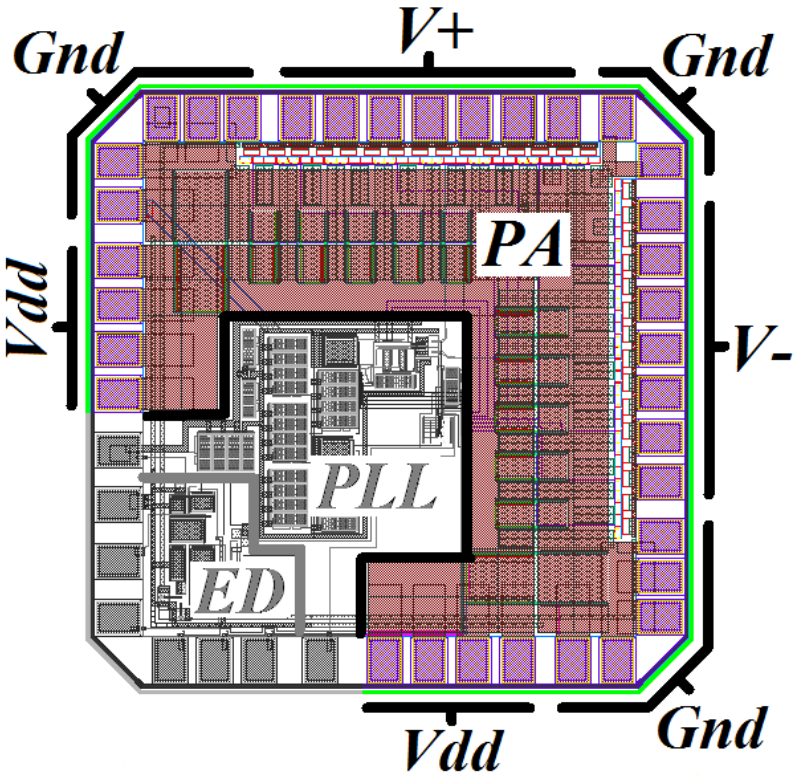
$$C_a = \frac{1}{\omega_o\left(\omega_o L_e - \sqrt{R_e(R_p - R_e)}\right)} \qquad C_b = \frac{1}{\omega_o R_p}\left(\sqrt{\frac{R_p}{R_e} - 1} - \sqrt{\frac{R_p}{R_s} - 1}\right)$$

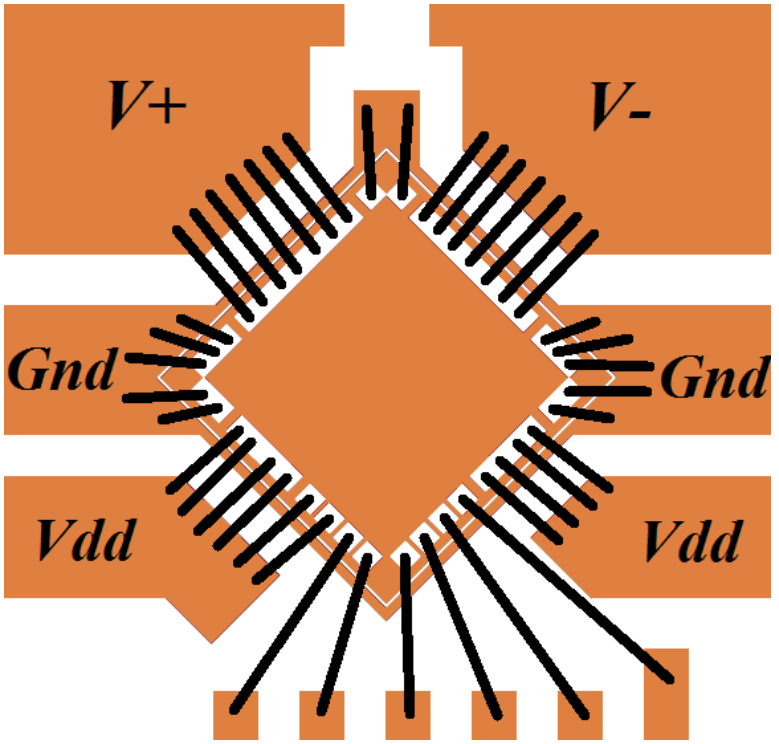
$$C_s = \frac{1}{\omega_o\sqrt{R_s(R_p - R_s)}}$$

Circuit implementation



Layout

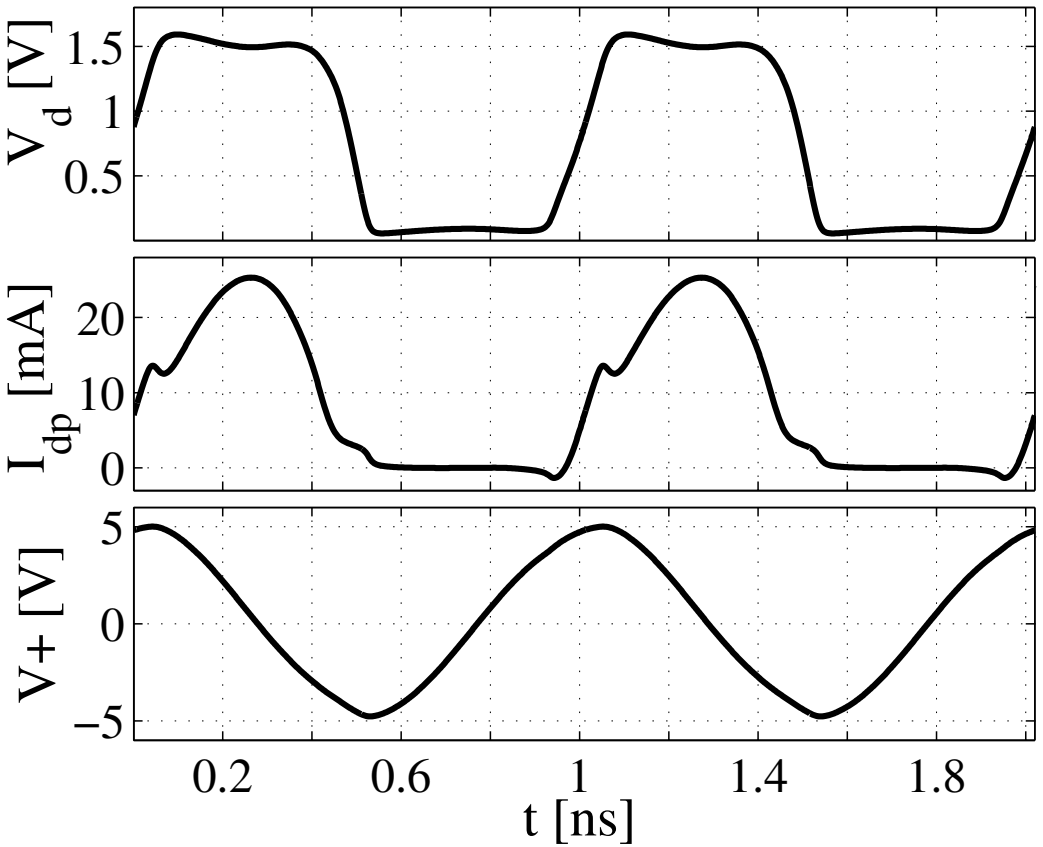




Die size: 2.25 mm^2

PA area: 1.5 mm^2

Simulation results

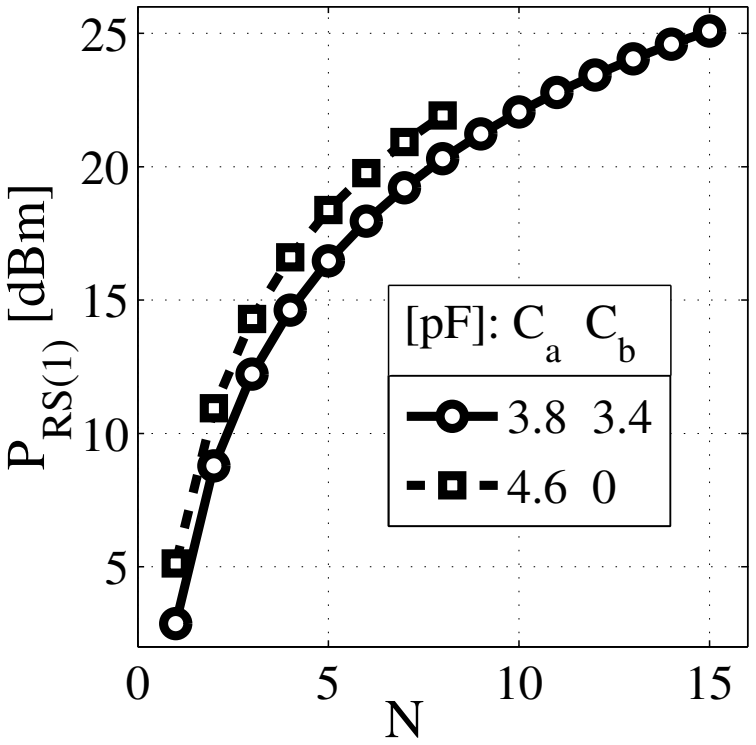


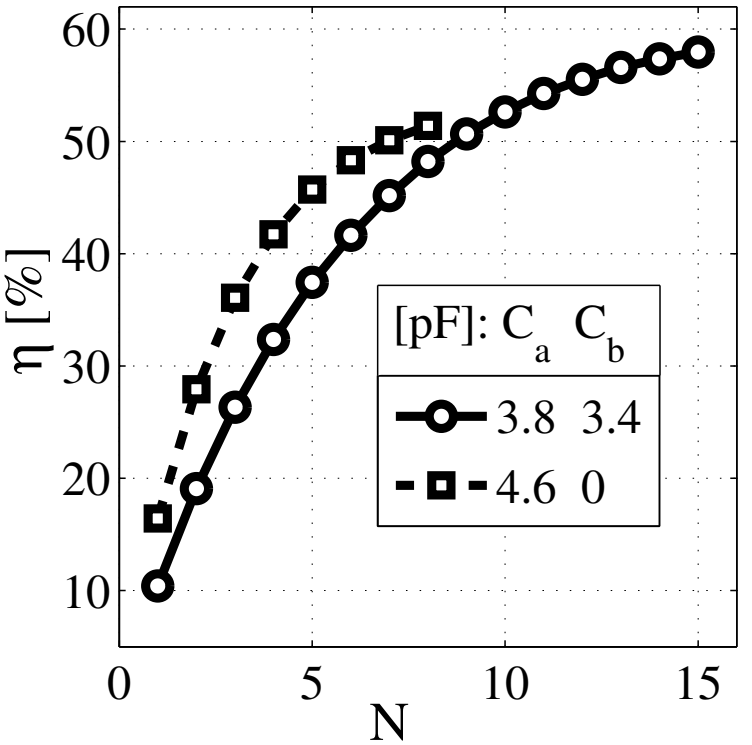
Drain voltage of the switches

Drain current at PMOS switch

Output node voltage

Simulated power and efficiency

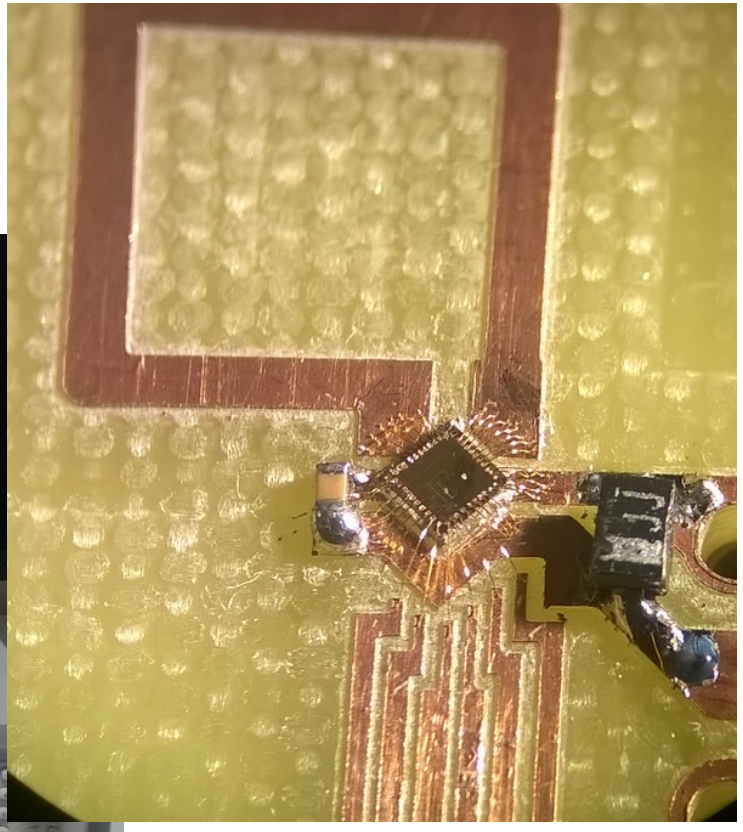




Summary of the PA designed

Technology	CMOS 180 nm
Frequency	990 MHz
Power	25.1 dBm
Efficiency	58%
PA load	1.8+j57.8
Area	1.5 mm^2
Integration level	High: only two external capacitors.
Configurability	Digitally controlled from 3dBm to 25dBm

Preliminary test



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- A design methodology is proposed to find the optimal width of the MOS transistors used as switches.
- The PA was divided into 15 unit cells allowing the individual enabling or disabling of each cell, in that way the output power can be digitally controlled.
- Post-layout simulations of the PA show that the maximum output power is 25.1 dBm with an efficiency of 58%.