Ultra-low-power 2.4 GHz Hartley oscillator

R. M. da Ponte and F. R. Sousa
RFIC Research Group - Electrical Engineering Department
Federal University of Santa Catarina
Florianopolis, SC, Brazil
Email: ronaldomponte@gmail.com, rangel@ieee.org

***Abstract*—This paper reports a design of an oscillator for ultra-low-power applications. The circuit was designed in a standard IBM 0.18 μm process and is based on the Hartley oscillator topology. Monte Carlo results showed that the oscillations are sustained with only 88 μW of DC power consumption from 1-V supply voltage and with a phase noise of -106.7 dBc/Hz at 1 MHz offset frequency, resulting in a FoM of 184.5 - which is suitable for ultra-low power applications.**

I. Introduction

The increasing demand in applications with limited power budget - such as implantable medical devices - requires circuits designed for ultra-low-power consumption with reasonable levels of signal integrity. Usually, these circuits have a radio-frequency system at the front-end in order to provide communication with the devices connected to a Wireless Body Area Network (WBAN) [1]. Oscillators are blocks that play a key role in a radio communication system, since they have to provide reference signals trading off high spectral purity and low power consumption. Thereby, in order to attend those particular demands, these circuits must be designed to best match with the aforementioned trade-offs.

Several former reports have discussed topologies and techniques to shrink both phase noise and power consumption in order to enhance the overall oscillator performance. In [2], an approach that consists in the optimizing of capacitor ratio is presented, which allows the circuit to work with supply voltages at only 20 mV. In [3], they employ a noise filter to reduce the phase noise of voltage controlled oscillators (VCOs) to its fundamental minimum according to the resonator quality factor and power consumption. The oscillators designed in [4] make use of a tail capacitance for filtering the current source noise altogether with a DC level shift that enables a large oscillation amplitude, while the core transistors operate in the saturation region. [5] presents a transformer-feedback VCO based on the concept of dual signal swings, allowing the output signals to swing above the supply voltage and below the ground potential, which increases the carrier power and decreases the phase noise. A similar idea is shown in [6], in which they replace the tail current of a traditional differential Colpitts VCO by inductors to augment the maximum attainable amplitude. In [7], the author uses a cross-coupled MOSFET pair with forward-body bias to boost the negative conductance of a millimeter-wave differential Colpitts oscillattor.

Undoubtedly, the current state-of-art of LC oscillators present an amount of techniques that upgrades the overall performance which is generally compared through the classical expression of figure-of-merit (FoM):

$$FoM = 20\log\frac{f_o}{\Delta f} - 10\log\frac{P_{DC}}{1mW} - L(\Delta f) \qquad (1)$$

where f_o is the oscillation frequency, P_{DC} is the DC power consumption and $L(\Delta f)$ is the phase noise at a Δf offset frequency. Nevertheless, the DC power consumption still revolves around a few miliwatts which could be unsuitable for some rigorous applications. This paper presents a design implementation of an ultra-low-power oscillator at 2.4 GHz which is suitable for demands that requires a DC power consumption under 100 μW. The oscillator is based on the classical Hartley topology and a prototype was designed in a standard 0.18 μm CMOS technology to verify the results. Post layout simulation outcomes indicate that the circuit oscilates at a frequency of 2.32 GHz reaching a DC power consumption of 88 μW from 1-V supply voltage and phase noise of -106.7 at 1 MHz offset frequency, which results in a figure-of-merit (FoM) of 184.5 dBc/Hz. Even though the phase noise has not presented the best result, which contributes to degrade the overall figure-of-merit, it is sufficient to comply with ZigBee specifications that require at least a -88 dBc/Hz phase noise at a frequency offset of 1 MHz from the carrier [8].

The rest of this paper is organized as follows: in section II, it is introduced a general circuit analysis; section III presents a design procedure focused on the passive network; section IV presents the circuit design; section V presents Monte Carlo and corners simulations in order to best estimate the sensibility of the design; and finally, section VI summarizes the most relevant contributions of this paper.

II. Circuit Analysis

There are many different approaches to realize the circuit analysis of an oscillator that can comprise negative resistance analysis and positive feedback loop, for instance. Irrespective of which analysis is chosen, all of them may converge for the simple Barkhausen criteria which dictates the required oscillation conditions for any feedback system.

Usually, the Hartley oscillator can be analysed by a general three-point oscillator approach presented by Figures 1(a) and 1(b). At this point of view, its small-signal equivalent circuit can be represented as showed in Figure 2 - in a very first order

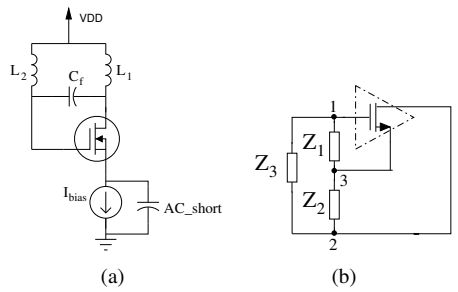


Fig. 1. Schematic diagram of designed oscillators: (a): Classical topology of Hartley oscillator; (b): Three-point oscillator equivalent circuit

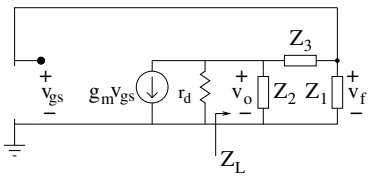


Fig. 2. Small-signal equivalent circuit

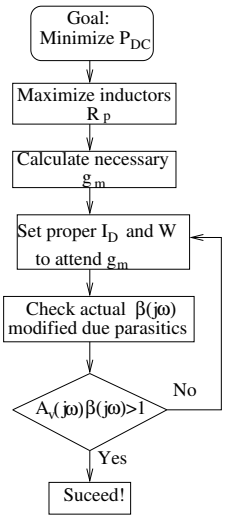


Fig. 3. Ultra-low-power oscillator design procedure flow chart

analisys. In this figure, r_d represents the output resistance at the drain, v_f the feedback voltage and Z_L the input impedance of the passive network composed by Z_1, Z_2 and Z_3. For $v_f = v_{gs}$, the direct and feedback gain can be expressed as:

$$A_v(j\omega) = \frac{v_o(j\omega)}{v_{gs}(j\omega)} = \frac{-g_m r_d Z_L}{Z_L + r_d} \tag{2}$$

$$\beta(j\omega) = \frac{v_f(j\omega)}{v_o(j\omega)} = \frac{Z_1}{Z_1 + Z_3} \tag{3}$$

Hence, the loop gain is given by:

$$A_v(j\omega)\beta(j\omega) = -\frac{g_m r_d Z_L Z_1}{(Z_L + r_d)(Z_1 + Z_3)} = \\ = -\frac{g_m r_d Z_1 Z_2}{r_d(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)} \tag{4}$$

Assuming that impedances Z_1, Z_2 and Z_3 are purely reactives and the phase of loop gain must be zero to sustain oscillations (i.e. $X_1(\omega_0) + X_2(\omega_0) + X_3(\omega_0) = 0$) , it can be shown that the loop gain can be expressed by:

$$A_v(j\omega_0)\beta(j\omega_0) = -\frac{g_m r_d X_1(\omega_0)}{X_1(\omega_0) + X_3(\omega_0)} = \frac{g_m r_d X_1(\omega_0)}{X_2(\omega_0)} \tag{5}$$

The loop gain must be greater than 1 to start oscillations, thus:

$$\frac{g_m r_d X_1(\omega_0)}{X_2(\omega_0)} > 1 \qquad \Longrightarrow \qquad g_m r_d > \frac{L_1}{L_2} \tag{6}$$

In other words, a transistor must be designed with a transcondutance that complies with the following requirement:

$$g_m > \frac{L_1}{L_2}(G_p + g_o) \tag{7}$$

Where g_o represents the output conductance and G_p the overall parallel loss of the passive network at the drain node. The oscillation frequency can be expressed as:

$$\omega_0 = 1/\sqrt{L_{eq} C_{eq}} \tag{8}$$

Where L_{eq} represents the equivalent inductance composed by L_1, L_2 and mutual inductances and C_{eq} the equivalent capacitance composed mainly by the feedback capacitor C_f of the passive network and the intrinsic capacitance C_{gd}.

III. Design procedure

As denoted in [7], it is necessary lower the equivalent parallel conductance of the passive network in order to reduce the power consumption. By this point of view, it is interesting to design inductors with the larger equivalent parallel resistance. Thus, the design procedure to be presented here has focused to maximize the equivalent parallel resistance R_p of inductors, in order to shrink the overall DC power. Since reaching large values for R_p is not a effortless task, it was chosen the same inductor value for L_1 and L_2. Once the equivalent R_p of the tank is set, a proper g_m transconductance must be calculated in order to cancel tank losses and start oscilations. A proper drain current I_D and a transistor width size W shall be set in order to attend the necessary g_m through the following relationship, assuming saturation regime:

$$g_m = \frac{2I_S(\sqrt{1 + i_f} - 1)}{n\phi_t} \tag{9}$$

Where $i_f \cong I_D/I_S$ is the inversion coefficient at the mosfet source terminal and I_S is the specific current which is directly proportional to the aspect ratio (W/L) and other technological parameters, n is the so-called slope factor and ϕ_t the thermal voltage [9]. At this point, some recursive iterations may be necessary since the mosfet might load in the node at L_2 with the intrinsic capacitances C_{gb} and C_{gs} which can slighty modify the feedback gain $\beta(j\omega)$. Once the modified feedback gain $\beta(j\omega)$ is checked and the product $A_v(j\omega_0)\beta(j\omega_0)$ is greater than 1, an oscillation can be sustained and a target reached. Figure 3 summarizes the ultra-low-power oscillator design through a simplified flowchart.

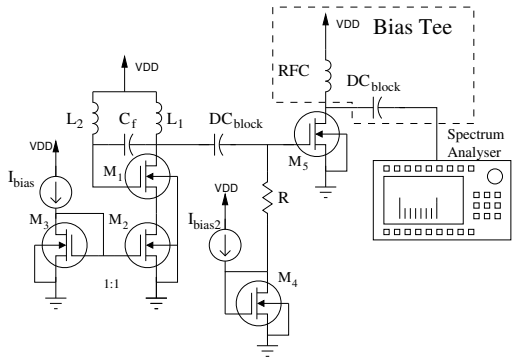


Fig. 4. Schematic of the ultra-low-power oscillator proposed

IV. Circuit Design

A protoype of the oscillator proposed was designed in the IBM 0.18 μm CMOS process in order to validade the results. The schematic of the circuit is presented in Figure 4 including a buffer stage at the oscillator output with the purpose to perform the measurements.

The circuit is current biased and a mirror was designed in order to yield a proper current reference and avoiding parasitic capacitance loading for the oscillator core. A buffer was designed in a common source stage in order to make possible the measurements. A large resistor (a few megaohms) was placed between gates of the buffer in order to prevent the output signal to be drained towards a low impedance path.

As already mentioned before, inductors size of L_1 and L_2 was designed to have the best R_p available in the process at the desired oscillation frequency. So, a proper drain current I_D and mosfet width size W was selected according to equation 9, in order to reproduce the required g_m necessary to start and sustain oscillations. After established these aforementioned parameters, a capacitor C_f is chosen taking into account the parasitic capacitance C_{gd} settle between gate and drain in order to produce an oscillation frequency at the vinicity of 2.4 GHz. Table I summarizes all component values used at the circuit design.

V. Simulation Results

This section presents the post-layout simulation results. Figure 6 depicts the layout of the proposed oscillator. The circuit was designed in Virtuoso Spectre Circuit Simulator from Cadence and sent to fabrication. Phase noise simulation was performed at 1 MHz offset frequency through the periodic steady state (PSS) analysis from Virtuoso Spectre Simulator. Table II and III shows the Monte Carlo and corner simulation results. Monte carlo simulation results were performed for 100 samples and include the maximum, minimum, mean and standard deviation for the figure-of-merit (FoM), oscillation frequency (f_o), DC power consumption (P_{DC}) and phase-noise at 1 MHz offset frequency. Corner simulation results presents the same aforementioned variables in seven different corners bounded by the process.

As can be seen, all corner simulation results passed successfully and the oscillator designed presented a FoM whose average is at 184.5 consuming only 88 μ W of DC Power. In Table IV the mean value of this work is compared with some state-of-the-art CMOS oscillators. Although the overall perfomance of this work has not fitted quite well, the DC power consumption has presented the best result of only 88 μW which is suitable for ultra-low power applications.

Soever the Monte Carlo simulations were performed for a specific operation point, a set of performances can be achieved by controling the supply voltage and/or the bias current. Figures 5(a) and 5(b) show the behaviour of overall performance (FoM) and phase-noise with changes in the supply voltage. As can be seen, the circuit reach its peak performance consuming 314 μW from 1.6-V supply voltage and presenting -116.1 of phase-noise at 1 MHz offset frequency which means a FoM of 189.1 dBc/Hz. Moreover, the operating frequency was initially designed at the vinicity of 2.55 GHz expecting that the parasitic capacitances - added at layout level - would slightly decrease it. Post-layout simulations showed that the circuit oscillates at the vinicity of 2.31 GHz,thus complying with the aforementioned assertion.

TABLE I
Component values

Component	Value	Unit
L_1	12.5	nH
L_2	12.5	nH
C_f	84	fF
R	561	kΩ
DC_{Block}	1	pF
W_1/L_1	60/0.18	μm/μm
W_2/L_2	500/0.19	μm/μm
W_3/L_3	500/0.19	μm/μm
W_4/L_4	1.76/0.18	μm/μm
W_5/L_5	18/0.18	μm/μm

TABLE II
Results of the Monte Carlo simulation (100 run)

Parameters	FoM (dBc/Hz)	f_o (MHz)	P_{DC} (μW)	L(1 MHz) (dBc/Hz)
Mean	184.5	2322	88.26	-106.7
Sigma	1.33	13.25	4.064	1.389
Max	188.3	2350	99.46	-103.4
Min	181.3	2274	78.19	-110.5

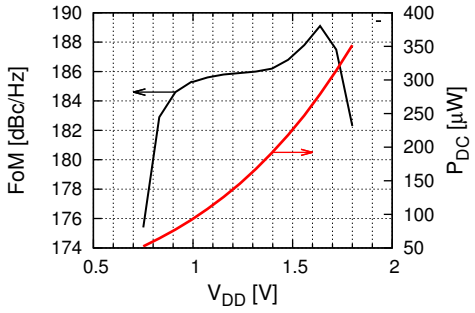
TABLE III
Results of corner simulations

Corners name	FoM (dBc/Hz)	P_{DC} (μW)	Frequency (GHz)	Phase-Noise (dBc/Hz)
Nominal	184.8	88.15	2.32	-106.9
ff	185.8	98.23	2.3	-108.3
fff	186.1	104.2	2.35	-108.8
fs	185.6	95.93	2.34	-108
sf	183.2	81.34	2.32	-105
ss	182.9	80.57	2.31	-104.7
ssf	181.2	77.14	2.3	-102.9

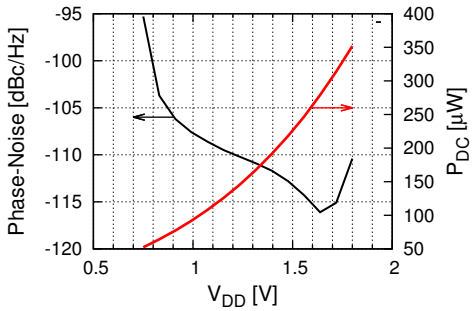
TABLE IV
COMPARISON BETWEEN STATE-OF-THE-ART CMOS OSCILLATORS

Parameters	[3]	[4] (RC bias)	[4] (TX bias)	[5]	[7]	This Work 1	This Work 2
CMOS Technology (nm)	350	130	130	180	130	180	180
Supply Voltage (V)	2.7	1.0	1.0	0.50	0.475	1.0	1.6
Frequency (GHz)	2.1	4.9	4.9	3.8	4.9	2.32	2.34
DC Power (mW)	9.3	1.4	1.3	0.57	2.7	0.088	0.314
Phase Noise (dBc/Hz)	-153^1	-132.8^1	-132.8^1	-119^2	-136.2^1	-106.7^2	-116.1^2
FoM (dBc/Hz)	195.4	195.5	196.0	193	196.2	184.5	189.1

[1] @ 3 MHz, [2] @ 1 MHz



(a)



(b)

Fig. 5. Performance comparison: (a): FoM and P_{DC}; (b): Phase-noise at 1 MHz of offset frequency and P_{DC}

VI. CONCLUSION

This paper presented an ultra-low-power oscillator for applications that requires a DC power consumption under 100 μW. A prototype was designed in IBM 0.18 μm process and monte carlo results showed that oscillator presents an oscillation frequency at 2.32 GHz with phase-noise of -106.7 dBc/Hz, consuming only 88 μW from 1-V supply voltage which indicates an FoM of 184.5 dBc/Hz. It is important to note that such ultra-low power was reached mainly due to the rigorous inductor design, which provided a large value for R_p allowed in the process. Thus, the necessary g_m required to cancel tank losses was significately reduced. Furthermore, the supply voltage can be increased in order to achieve better overall performances, which implies in an increased power consumption.

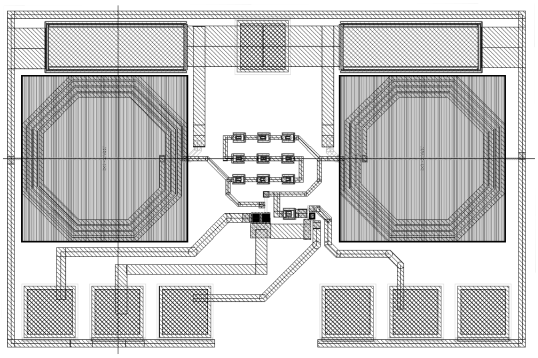


Fig. 6. Layout of the oscillator

VII. ACKNOWLEDGMENTS

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