Modeling and Design of High-Efficiency Power Amplifiers Fed by Limited Power Sources

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***Abstract*—Recently the non-electromagnetic energy sources and wireless power transfer (WPT) techniques have been used to obtain electromagnetic (EM) energy sources for providing energy autonomy to electric devices when the energy in the environment is insufficient. Typically, this type of systems are composed by a harvester, a DC/RF converter, a WPT interface and a load. Further, in the power stage of the DC/RF converter the energy flow is processed using a power amplifier (PA). This paper proposes a design methodology for a generic PA fed by a limited power source. This methodology extracts the maximum available power of the EPS with the maximum PA efficiency using impedance matching and a novel PA modeling based on its impedance ports (DC and AC). Moreover, models of class-A PA and class-D PA were developed as examples. Furthermore, a Class-A PA was designed using its impedance ports model and the proposed methodology as a proof of concept. The results reflect that the designed PA extracts the maximum available power of the source with its maximum efficiency.**

***Keywords*—Class-A power amplifier, class-D power amplifier, efficiency, power amplifier modeling, wireless power transfer.**

I. Introduction

Currently, there is an increasing interest in providing energy autonomy to electric devices (e.g. sensors) in order to implement concepts such as the Internet of Things (IoT), and Wireless Body Area Networks (WBAN) [1]–[3]. Energy-harvesting technologies allow this autonomy, collecting energy from primary energy-sources (i.e. solar, thermal, kinetic, or electromagnetic) and converting it to DC power using a transducer. This system can be modeled using the energy power source (EPS) concept proposed in [4]. Following this modeling approach, the system composed by the primary energy source (e.g. solar) and the harvester (e.g. photovoltaic cell) can be considered as a Power EPS, that means, it supplies a high amount of energy (i.e. self-sustaining), but it has a weak power density and cannot sustain a stable output voltage under loading conditions [5].

When the energy in the environment is insufficient a self-sustaining WPT system can be used as a secondary energy source for powering an self-sustaining device [6]. A typical self-sustaining WPT system is illustrated in Fig. 1, it is composed by a power EPS, DC/RF converter (i.e. oscillator and power amplifier, or power oscillator), a WPT interface (i.e. antenna or inductive link), and a load. For instance, in [7] it is proposed a self-sustaining WPT as an additional EM energy source when there is availability of solar light but limited EM signals in the environment. This system was based on photovoltaic cells, class-E oscillator (905 MHz), and monopole antenna. The measured efficiency of the DC/RF converter was 43%. In general, given that the system EPS is a power EPS the efficiency of the overall power-chain (i.e. the circuit used for processing the energy flow from primary source to the load) must be very high [8].

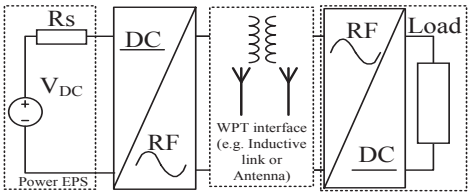


Fig. 1. Simplified block diagram of a self-sustaining WPT system

In the traditional design approach of self-sustaining devices the interactions among EPSs, converters and loads are reduced to a specification (i.e. a voltage or a current) between the subsystems. Then they are optimized individually using this specification as a constraint. For example, in [5] a voltage specification of 1.9 V is imposed by design, then the power EPS (a regulated voltage source based on multi-harvest EPSs) was optimized for the extraction of the maximum available power. The self-sustaining voltage source, proposed by [9], for powering smart nodes of IoT is another example of this design approach. This EPS achieves low power operation and a high efficiency for the predefined voltage specification (3.3V), and imposes this voltage as a constraint for the load design.

For the self-sustaining WPT system, the traditional design approach of self-sustaining devices is inadequate, because it does not maximize the power delivered to the load. Further, the designer can improve the system performance by optimizing both the trade-offs and the interactions within the circuits. For instance, a non regulated voltage between the EPS and the power amplifier (PA) was explored in [10]. They proposed a regulator-less PA with an adaptive output matching network for maintaining the load power constant while the supplied voltage decreases. With this approach the overall system efficiency was increased and the burst time of a wireless sensor network node was maximized. However, this technique increases the hardware complexity. On the other hand, the harmonic balance optimization, proposed by [7], maximizes the conversion efficiency of the power oscillator without penalty on the system complexity, but it is limited to a specific harvester condition.

This paper proposes a methodology for maximizing the

output power of a PA fed by a power EPS without an increase of the circuit complexity. It extracts the maximum available power of the EPS (P_{avs}) with the maximum PA efficiency using impedance matching and a novel PA modeling based on its impedance ports (DC and AC).

II. Application Context: The WPT Node Concept

The PA analyzed in this paper is part of a self-sustaining WPT system for transferring energy from a WBAN node to an implanted device as shown in the Fig. 2. In order to achieve energy autonomy, the WPT system harvests energy from the body environment (e.g. solar and thermal), then it is transferred through an inductive link to the implanted device. The simplified system block diagram is shown in Fig. 3(a). The inductive link uses the magnetic coupling between two inductors: the primary inductor (L_1) is connected to the source and the secondary (L_2) is embedded into an implanted device. This inductive link is expected to operate under weak coupling regime, for this reason, the load of the DC/RF converter may be approximated as the impedance of primary inductor. A generic linear power EPS was modeled using a resistor (R_s) and a ideal voltage source (V_{DC}), the R_s captures both the limited power characteristic of the EPS and the output voltage drop when it is loaded.

III. Energy Power Supply (EPS)

The EPS energy (E_s) is supplied by the combination of current (i_s) and voltage (v_s) with an energy rate (P_s) given by:

$$P_s(t) = \frac{dE_s(t)}{dt} = v_s(t)\, i_s(t)\,. \tag{1}$$

An ideal EPS must deliver an infinite energy at a required load power, in a small form factor [4]. On the contrary, any real EPS delivers a limited energy at a limited power with a specific form factor [4]. When an EPS is based on energy harvester, it supplies a high amount of energy, but at a limited low power [8]. Additionally, this maximum power value (P_{avs}) can be extracted only when the power transfer condition is satisfied. On the other hand, when the EPS is based on an energy carrier (e.g. battery), it supplies a high power during a limited time, because it has a limited energy-storage-capacity (E_{st}). In [4] a taxonomy based on the E_{st} and the P_{avs} EPS characteristics was proposed, it is summarized in Table I.

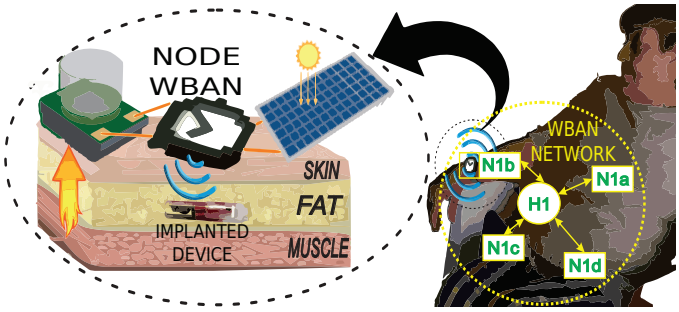


Fig. 2. Self-sustaining WPT system for powering implanted device.

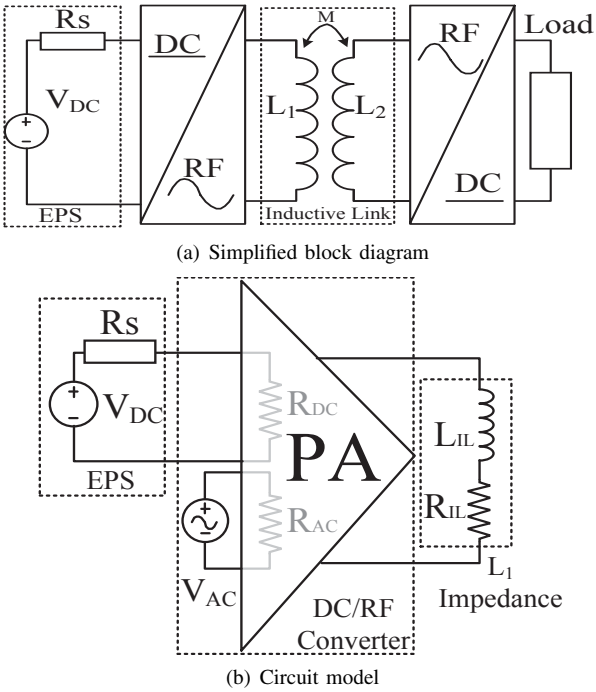


Fig. 3. WPT system for powered an implanted device

TABLE I. EPS taxonomy based on [4]

EPS Name	P_{avs}	E_{st}	Example
Ideal EPS	infinite	infinite	The sun
Real EPS	finite	finite	Electric distribution network
Power EPS	low	high	Solar Energy + PV cell
Energy EPS	high	low	AAA battery

IV. PA Modeling

A. Modeling of the energy-flow process using the PA impedance ports

Assuming a DC/RF converter based on an oscillator that drives a PA as shown in Fig. 3(b), the energy flows from the the DC source (V_{DC}) and the AC source (V_{AC}) to the load ($R_L = R_{IL}$) connected to the RF port. In order to model the energy-flow process in the PA, equivalent resistances in its input ports are proposed: R_{DC} in the PA DC-port and R_{AC} in the PA AC-port, as depicted in Fig.4(b). Some of power "disipated" in R_{DC} and R_{AC} is transfered to the load. Considering resonant load, narrow-band operation, and ideal passive elements, the load power in steady state depends only on the external elements connected to the PA, therefore the load port could be considered as a power source. This circuit element imposes the power on its load [11], the I–V characteristic of the a DC power source of 1W is illustrated in Fig.4(b). Using this model, the current (I_{RF}) and the voltage (V_{RF}) in the RF port are imposed by both the load and the power source, and are given by:

$$I_{RF} = I_m sin\,(\omega_0 t)\,; \tag{2}$$
$$V_{RF} = V_m sin\,(\omega_0 t)\,; \tag{3}$$

where, I_m is the peak load current, V_m is the peak load voltage, and ω_0 is the natural frequency of the resonant load (i.e. C_0,L_0

and R_L). In addition, the power delivered to the load (P_{RF}), the power supplied by the DC source (P_{DC}), and the the power supplied by the AC source (P_{AC}) are given by:

$$P_{RF} = \frac{{I_m}^2}{2} R_L = \frac{{V_m}^2}{2R_L} = \frac{I_m \cdot V_m}{2}; \tag{4}$$

$$P_{AC} = \frac{\omega_0}{2\pi} \int_0^{\frac{2\pi}{\omega_0}} i_{AC}(t) \cdot v_{AC}(t) \cdot dt; \tag{5}$$

$$P_{DC} = {I_{DC}}^2 R_{DC} = \frac{{V_{DC}}^2}{R_{DC}} = I_{DC} V_{DC}; \tag{6}$$

where, R_L is the load impedance at resonance, i_{AC} is the current supplied by the AC source, v_{AC} is the voltage supplied by the AC source, I_{DC} is the DC current supplied by the EPS, V_{DC} is the voltage supplied by the EPS, and R_{DC} is the impedance imposed by the amplifier in its DC-port.

B. PA efficiency predicted by the PA model based on its impedance ports

The power "disipated" in R_{DC} and R_{AC} and transfered to R_L (P_{RF}) can be calculated following the power added efficiency (PAE) definition (7). On the other hand, following the drain (or colector) efficiency (η_D) definition, P_{RF} could be calculated as (8). Further, following the PA efficiency (η) definition the P_{RF} is given by (9).

$$P_{RF} = PAE \cdot P_{DC} + P_{AC}; \tag{7}$$

$$P_{RF} = \eta_D \cdot P_{PA}; \tag{8}$$

$$P_{RF} = \eta \cdot (P_{DC} + P_{AC}); \tag{9}$$

where, P_{DC} is supplied by the DC source (V_{DC}), P_{AC} is supplied by the AC source (V_{AC}), and P_{PA} is the power consumed by the PA power stage. When the P_{AC} is negligible compared to P_{DC}, the value of PAE, η_D and η are equal. Hence they can be approximated by (10). Using (4) and (6), the equation (10) can be rewritten as (11).

$$\eta \approx PAE \approx \eta_D \approx \frac{P_{RF}}{P_{DC}}; \tag{10}$$

$$\eta = \frac{R_L}{2R_{DC}} \left(\frac{I_m}{I_{DC}} \right)^2. \tag{11}$$

The power delivered by V_{DC} is consumed by both the bias circuit (or the driver circuit) and the PA power stage, therefore the I_{DC} is given by (12). Using (12) the R_{DC} can be calculated by (13).

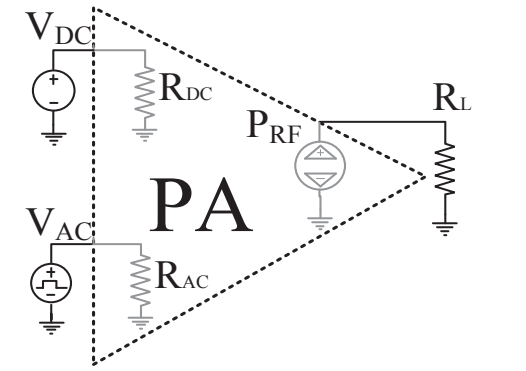
$$I_{DC} = I_{bias} + I_{PA} = \frac{R_{PA} \cdot I_{PA}}{R_{bias}} + I_{PA}; \tag{12}$$

$$R_{DC} = \frac{V_{DC}}{I_{DC}} = R_{bias} \| R_{PA}; \tag{13}$$

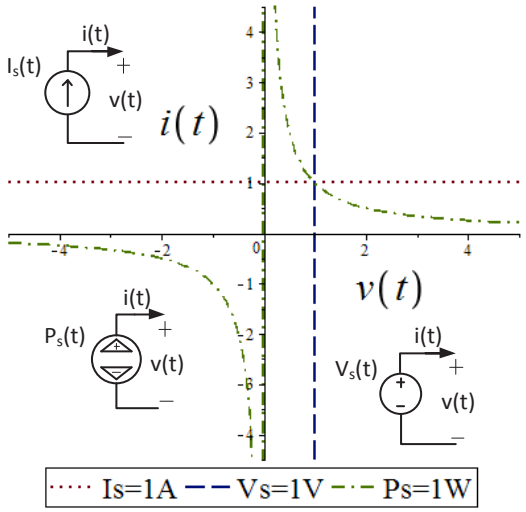
where, I_{bias} is the DC current of the bias circuit, I_{PA} is the DC current of the PA power stage, R_{bias} is the resistance imposed by the bias circuit to the DC source and R_{PA} is the resistance imposed by the PA power stage to the DC source. Hence, using (12) and (13) the equation (11) can be rewritten as (14).

$$\eta = \frac{1}{2} \frac{R_L R_{DC}}{{R_{PA}}^2} \left(\frac{I_m}{I_{PA}} \right)^2 = f(G_R); \tag{14}$$

where, G_R is the PA impedance factor defined as $G_R = R_{DC}/R_L$, and $f(x)$ is a function dependent on the PA topology. The PA efficiency is maximum for an optimum relationship between its port impedances (i.e. $G_R = G_{R_{opt}}$). In the next subsections we discuss the models of class-A PA and class-D PA based on its impedance ports as examples of the proposed modeling technique.



(a) PA Model



(b) Power source example

Fig. 4. PA Model based in its port resistors and a controled power source.

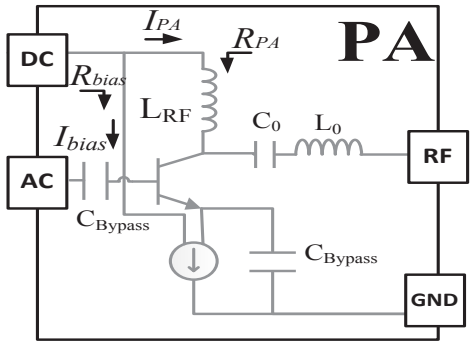
C. Example 1: BJT class-A PA

Considering the schematic shown in the Fig. 5(a), a negligible energy consumption of the bias circuit (i.e. $R_{DC} \approx R_{PA}$) and (14), the η can be expressed as:

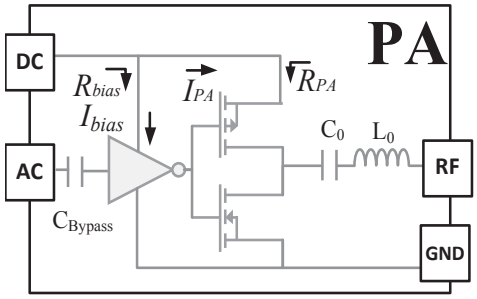
$$\eta \approx \frac{0.5R_L}{R_{PA}} \left(\frac{I_m}{I_{PA}} \right)^2 \approx \frac{0.5R_L}{R_{DC}} \left(\frac{I_m}{I_{DC}} \right)^2. \tag{15}$$

Considering the exponential model of the BJT transistor presented in [12], (15) can be rewritten as:

$$\eta = \frac{1}{2G_R} {h_i}^2 \left(\frac{|v_{ac}|}{\phi_t} \right); \tag{16}$$



(a) Class-A PA



(b) Class-D PA

Fig. 5. Analyzed PA topologies.

where, $|v_{ac}|$ is the peak voltage value of the sinusoid input signal (V_{AC}) normalized by the thermal voltage (ϕ_t) and the function $h(x)$ is given by:

$$h\left(x\right) = 2\frac{I_1\left(x\right)}{I_0\left(x\right)}; \tag{17}$$

where, $I_n(x)$ is the modified Bessel function of the first kind, of order n and argument x. The PA operates as class-A PA until I_m is equal to the I_{PA} or V_m is equal to the Collector bias voltage (V_C). Therefore, in order to achieve the class-A operation (i.e. $I_m < I_{PA}$ and $V_m < V_C$) the $|v_{ac}|$ value must be lower than a maximum value given by:

$$\left|v_{ac}\right|_{\phi_t M} = \begin{cases} h^{-1}\left(1\right) \approx 1.16 & G_R > 1; I_m = I_{PA} \\ h^{-1}\left(G_R\right) & G_R < 1; V_m = V_C \end{cases}; \tag{18}$$

where, $h^{-1}(x)$ is the inverse function of the $h(x)$. Finally, from (16) and (18) the PA efficiency is given by :

$$\eta = f_{A_{BJT}}\left(G_R\right) = \begin{cases} 0.5 \cdot G_R & G_R < 1 \; ; \Rightarrow I_m = I_{PA} \\ \frac{1}{2G_R} & G_R \geq 1; \Rightarrow V_m = V_C \end{cases}. \tag{19}$$

This efficiency is maximum when $G_R = G_{R_{opt}} = 1$ is forced by design. In this case, the maximum value of $\eta = f_{BJT}\left(G_{R_{opt}}\right)$ is 50%.

D. Example 2: CMOS class-D PA

Considering the schematic shown in the Fig. 5(b), ideal components, pulse signal of 50% of duty cycle in the PA AC-port, assuming a resonant load with high loaded quality factor, modeling the MOSFET (N and P type) as an ideal switch and a series resistance (R_{on}), I_m can be approximated by (20). Additionally, the current waveform of the PA power stage is a rectified sinusoid with peak value of I_m, therefore its average value (I_{PA}) is given by (21). Further, using (20) and (21) the impedance imposed by the PA power stage (R_{PA}) can be calculated as (22). Moreover, the power used to charge and discharge the total gate capacitances of the MOSFETs (C_G), dissipated by the driver, could be modeled with an equivalent resistance (R_{bias}) given by (23).

$$I_m = \frac{V_m}{\left(R_L + R_{on}\right)} = \frac{4V_{DC}}{\pi\left(R_L + R_{on}\right)}; \tag{20}$$

$$I_{PA} = 2I_m/\pi; \tag{21}$$

$$R_{PA} = \frac{V_{DC}}{I_{PA}} = \frac{\pi^2}{8}\left(R_L + R_{on}\right); \tag{22}$$

$$R_{bias} = \frac{{V_{DC}}^2}{P_{bias}} \approx \frac{{V_{DC}}^2}{{V_{DC}}^2 \cdot f \cdot \alpha \cdot C_G} = \frac{1}{f \cdot \alpha \cdot C_G}; \tag{23}$$

where, the factor α represents the capacitance excess due to the driver implementation and f is the frequency of the AC input. The $C_G \cdot R_{on}$ product could be considered quasi constant and given by the product of two technology parameters (i.e. a and b) introduced in [13], hence (23) can be rewritten as (24). From (22) and (24) the G_R can be calculated by (25).

$$R_{bias} = \frac{R_{on}}{f \cdot \alpha \cdot a \cdot b}; \tag{24}$$

$$\frac{1}{G_R} = \frac{R_L}{R_{DC}} = \frac{f \cdot \alpha \cdot a \cdot b}{\frac{R_{on}}{R_L}} + \frac{8}{\pi^2}\frac{1}{\left(1 + \frac{R_{on}}{R_L}\right)}. \tag{25}$$

From (14), (21) and (22), the η can be calculated by:

$$\frac{1}{\eta} = \frac{\pi^2}{8} \cdot \frac{1}{G_R} \cdot \left(1 + \frac{R_{on}}{R_L}\right)^2. \tag{26}$$

Using (25), the equation (26) can be rewritten as:

$$\eta = f_{D_{CMOS}}\left(\mathrm{G}_R\right) = \frac{1}{\left(1+l(\mathrm{G}_R)\right)\left(1+k\left(1+\frac{1}{l(\mathrm{G}_R)}\right)\right)}; \tag{27}$$

where $k = \frac{\pi^2}{8}\alpha \cdot a \cdot b \cdot f$ and the function $l(x)$ is given by:

$$l\left(x\right) = \tfrac{1}{2}\left(\left(A+B\right)x - 1 \pm \sqrt{1 + \left(2A - 2B\right)x + \left(A+B\right)^2 x^2}\right); \tag{28}$$

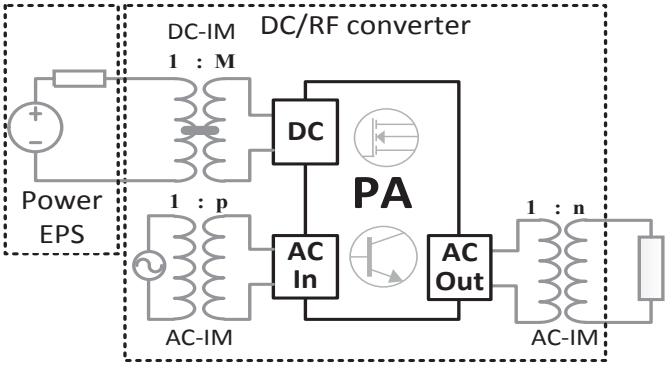
where, $A = f \cdot \alpha \cdot a \cdot b$ and $B = \frac{8}{\pi^2}$. This efficiency is maximum when (29) is forced by design. In this case, the maximum value of η is given by (30).

$$l\left(\mathrm{G}_{R_{opt}}\right) = \sqrt{\frac{k}{k+1}} \tag{29}$$

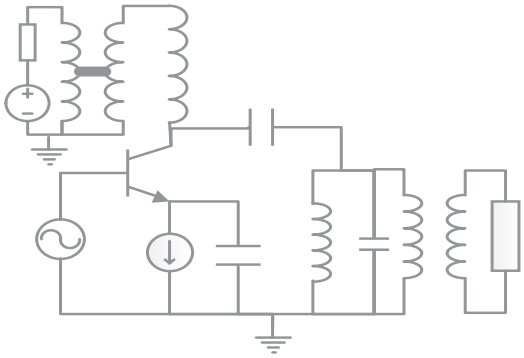
$$f_{D_{CMOS}}\left(G_{R_{opt}}\right) = \frac{\sqrt{k^2+k}}{\left(k + \sqrt{k^2+k}\right)\left(k + 1 + \sqrt{k^2+k}\right)}. \tag{30}$$

V. PA Design Methodology

In the application described in Fig. 2, the design goal is to maximize the power delivered to the load (R_{IL}). This methodology achieves this goal by the maximization of both the power supplied by the harvester and the PA efficiency. Therefore, the methodology finds the optimum R_{DC} ($R_{DC_{opt}}$) that dissipated the P_{avs} of the power EPS at the highest possible voltage for a particular implementation. Following, the methodology finds the optimum R_L ($R_{L_{opt}}$) based in the



(a) General



(b) Class-A

Fig. 6. DC/RF converter topologies with impedance matching networks

calculated $R_{DC_{opt}}$ and the $G_{R_{opt}}$ of the used PA topology. In particular the $G_{R_{opt}}$ (calculated using (19) and (27)) of the analyzed PAs in Section IV is summarized in Table II. Finally, the $R_{DC_{opt}}$ is matching to the power EPS impedance by a DC IM network (DC-IM) and the $R_{L_{opt}}$ is matching to the impedance of the real load by a AC IM network (AC-IM), as is illustrated in Fig 6(a). These networks was modeled as an ideal transformers (i.e. assuming IM networks with negligible losses). Further, the DC-IM implementation could be an DC/DC converter, and the AC-IM implementation could be a L or π network. The design methodology steps were proposed and summarized in Table III. The application of this methodology is illustrated in Section VI.

TABLE II. G_{opt} FOR THE ANALYZED PAS

BJT ClassA PA	CMOS ClassD PA
1	$\frac{\sqrt{(k+1)k}+k}{(A+B)\sqrt{(k+1)k}+A(k+1)}$ $k=\frac{\pi^2}{8}\alpha\cdot a\cdot b\cdot f$ $A=f\cdot\alpha\cdot a\cdot b$ and $B=\frac{8}{\pi^2}$

VI. PA STUDY CASE

In order to verify (19) experimentally, a class A PA (Fig. 6(b)) was designed, simulated and implemented. The

TABLE III. DESIGN METHODOLOGY STEPS

Step	Step Description	Equation
1	Find the P_{avs} of the power EPS and its related variables: optimum load impedance (R_{pavs}), load voltage (V_{pavs}) and current (I_{pavs}).	e.g. for a thermoelectric generator, the internal series resistor of the EPS (R_s) is constant, therefore: $R_{pavs}=R_s$, $V_{pavs}=\frac{V_{DC}}{2}$ and $I_{pavs}=\frac{V_{DC}}{2R_s}$.
2	Fix the voltage in the PA DC-port as the highest for a particular implementation restriction, e.g. the technology voltage of the CMOS process.	$V_{DC_{opt}}=V_{\max}$
3	Find the DC current that extracts the P_{avs} of the EPS	$I_{DC_{opt}}=\frac{P_{avs}}{V_{\max}}$
4	Find the impedance of the PA DC-port that maximizes the power extracted from the harvester.	$R_{DC_{opt}}=\frac{V_{DC}}{I_{DC}}=\frac{V^2_{\max}}{P_{avs}}$
5	Find the optimum load value for maximizing PA efficiency	$R_{L_{opt}}=G_{R_{opt}}R_{DC_{opt}}$
6	Find the specifications of the DC and AC impedance matching networks (DC-IM and AC-IM).	$M=\sqrt{\frac{R_{DC_{opt}}}{R_{p_{avs}}}}=\sqrt{\frac{V^2_{\max}}{P_{avs}\cdot R_{p_{avs}}}}$ $n=\sqrt{\frac{R_L}{R_{L_{opt}}}}=\sqrt{\frac{P_{avs}\cdot R_L}{G_{R_{opt}}V^2_{\max}}}$

amplifier design specifications are summarized in Table IV. The simulation setup uses the harmonic balance simulation technique in the Advanced Design System (ADS®) software. Furthermore, two parametric sweeps, the input signal (V_{AC}) sweep and the R_{PA} sweep, were implemented. The R_{PA} sweep was implemented by a fixed current (I_{PA}=1mA) and a V_{DC} sweep. Additionally, the circuit was simulated with and without the output LC tank filter. Further, the assumption that P_{AC} is negligible compared to P_{DC} was verified (i.e. $P_{AC}<8\mu$W for all simulations). The simulation results are summarized in Table V.

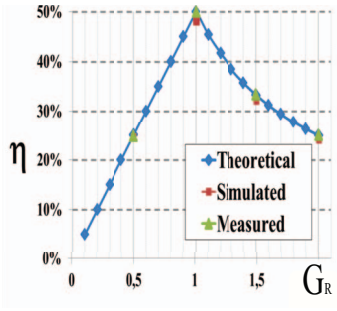
The PA was implemented without the output LC tank and the fundamental components were obtained by FFT processing on the time-domain signals in order to avoid the influence of the parasitic elements of the LC tank. In the experimental setup (Fig. 7b), the I_{PA} was fixed to 1 mA and the R_{DC} was set with the V_{DC}. In this setup, V_{AC} was incremented until the PA operates at the limit of the class-A operation ($I_m=I_{PA}$ or V_m=V_C). At this point the efficiency was calculated through the measured values (i.e. I_{PA}, V_{DC}, and V_m). The voltage operation limit ($V_m=V_C$) was measured with a digital oscilloscope with FFT option. On the other hand, the voltage

TABLE IV. PA SPECIFICATIONS

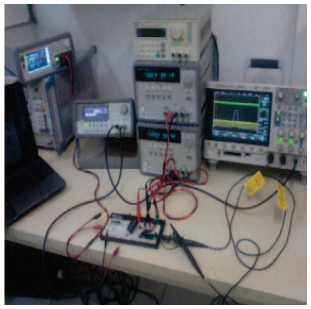
V_{DC}	I_{PA}	f	$R_{L_{opt}}$
1V	1mA	100 kHz	1kΩ

TABLE V. PA SIMULATION RESULTS

R_{PA} (Ω)	Limit type	$\lvert v_{ac}\rvert_{\phi_t}$	P_{DC} w/o_LC (mW)	P_{DC} w_LC (mW)	P_L w/o_LC (mW)	P_L w_LC (mW)	η w/o_LC (%)	η w_LC (%)
0.5	V_m=V_C	0.530	0.564	0.564	0.138	0.138	24.5	24.5
1.0	V_m=V_C	1.181	1.127	1.127	0.545	0.545	48.3	48.2
1.5	I_m=I_{PA}	1.180	1.691	1.691	0.545	0.545	32.2	32.1
2.0	I_m=I_{PA}	1.180	2.254	2.254	0.545	0.545	24.2	24.1



(a) Efficiency results



(b) Experimental setup

Fig. 7. Implemented class-A PA

operation limit ($I_m = I_{PA}$) was estimated from the V_m and the measured load value (R_L= 997.74 Ω). The experimental results are summarized in Table VI. The predicted efficiency by the model and the results (simulated and experimental) are plotted in the Fig. 7a, considering this figure, the equation (19) is an appropriate expression for model η.

In order to verify experimentally the proposed methodology without the practical limitations of the commercial harvesters and the impedance matching networks (AC and DC), we choose a scenario with the following specifications: a power EPS with $P_{avs} = 1$mW and $R_{pavs} = 1$kΩ, a resistive load of $R_L = 1$kΩ, and an ideal sinusoid input signal with the required amplitude and frequency of 100kHz. The specifications of the PA and the IM networks were calculated following the methodology steps listed in the Table III. The results are summarized in Table VII. In the experimental setup, the AC input was incremented until the PA operates at its maximum efficiency. The DC/RF converter efficiency was calculated through the measured values, and the EPS efficiency was calculated based on its DC current and the output open voltage. The results are summarized in Table VIII. They reflect that the designed converter extracts the P_{avs} of the power EPS with the maximum PA efficiency (i.e. 50%).

VII. Conclusions

A design methodology for a generic PA fed by a power EPS was proposed. Using this methodology, a class-A PA was designed, implemented and tested. The results reflect that the designed PA extracts the maximum available power of the source with its maximum efficiency. Further, the PA modeling based on its impedance ports (DC and AC) was proposed. Furthermore, the models of class-A PA and class-D PA were developed as examples of the proposed modeling technique. Also, this paper presents an open challenge on EPSs, Energy converters (i.e. PAs) and circuits that could take advantage of the use of power specifications instead of predefined voltage or current condition between them.

TABLE VI. PA experimental results

R_{PA} (Ω)	Limit type	$\lvert v_{ac}\rvert_{\phi_t}$	LC tank	P_{DC} (mW)	P_L (mW)	η (%)
0.50	V_m=V_C	0.679	w/o	0.5002	0.1242	24.8
1.00	V_m=V_C	1.516	w/o	10.003	0.5004	50
1.50	I_m=I_{PA}	1.516	w/o	15.002	0.5010	33.3
2.00	I_m=I_{PA}	1.516	w/o	2.002	0.5010	25

TABLE VII. DC/RF converter specifications

$V_{DC_{opt}}$	$I_{DC_{opt}}$	$R_{DC_{opt}}$	$R_{L_{opt}}$	M	n
1V	1mA	1kΩ	1kΩ	1	1

TABLE VIII. DC/RF converter experimental results

R_{DC}	P_{EPS}	P_{DC}	P_{RF}	η_{EPS}	$\eta_{DC/RF}$
1.001kΩ	2.004mW	1000.3 μW	500.4μW	50%	50 %

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