A miniaturized low-power radio frequency identification tag integrated in CMOS for biomedical applications

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***Abstract*—Biomedical implant miniaturization is one of the trends that have appeared recently for health monitoring to overcome size limitations and therefore reach restricted body areas. RFID technology can be used as a tool, due to its biocompatibility with human body and non-invasive measurement capacity, as long as it is directed to miniaturization. This work presents a low-power miniaturized near-field RFID tag operating at 1.04 GHz in a standard CMOS 180 nm technology inside an available area of 1.5 mm × 1.5 mm. An internal ROM and corresponding reading circuit was included so as to emulate information stored in the tag. The layout-extracted simulations proved that the tag backscatters a 1 MHz amplitude-modulated signal when powered at -4 dBm.**

I. Introduction

Nowadays, Radio Frequency Identification (RFID) is one of the main technological tools used for object identification, access management and tracking of people and animals, among many others applications. Different fields have incorporated the use of this technology for time optimization and constant monitoring such as product tracking, inventory control, supply-chain processes, biomedical applications and transport ticketing integration [1].

Furthermore, with the evolution of the integrated circuits and the wireless technologies, a modern concept has emerged: "The Internet of Things" (IoT). Its main objective is to extract massive real-time information from smart devices through a global network, process and evaluate the data in a colossal database and take new decisions without human intervention. By integrating RFID to IoT, new applications can be envisaged such as natural disaster predictions, proper farming monitoring methods [2] and biomedical implants [3]. Particularly, the research efforts in this latter area have evolved considerably in the last years with RFID miniaturization, due to space-body limitation. These high-frequency biomedical implants must be redirected to fully integrated systems in order to achieve restricted body areas. The on-chip tag antenna is one of the main components that has been investigated recently in the interest of reducing the implants size [4].

High quality factor inductor studies were realized in order to reduce losses and therefore increase its efficiency [5]. A 1.04 GHz integrated receiver with on-chip inductor was proposed in a 1.5 mm × 1.5 mm area [6]. In order to develop a biomedical application, new circuits must be defined to sense, acquired and transmit information from the body to the monitoring network.

Therefore, this work complements the work in [6] by implementing a miniaturized low power battery-less fully-integrated memory reading circuit for biomedical implant applications, as presented in Fig. 1, in a 1.5 mm × 1.5 mm area. A full-custom Read Only Memory (ROM) is accessed and its contained information is transmitted using load modulation with a 1 MHz backscattering signal to an RFID reader.

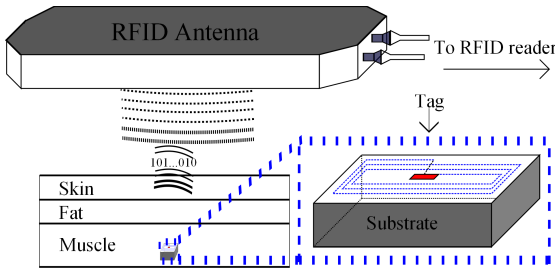

Fig. 1. Energy and information exchange between the RFID reader and the implanted tag.

II. Description of the Main Blocks

A. Miniaturized inductor

A full-custom one-turn planar inductor [6] with a 250 μm linewidth and 1.21 mm average diameter was implemented in the uppermost metal level of the CMOS technology. The design procedure objective consists in maximizing the quality factor of this inductor in order to reduce the energy losses, which is important due to the small amount of power received by this component. The designed inductor is presented in Fig. 2 with its corresponding substrate.

B. ROM Reading circuit

The blocks diagram of the proposed circuit is presented in Fig. 3 and it is composed by combinational and sequential digital logics.

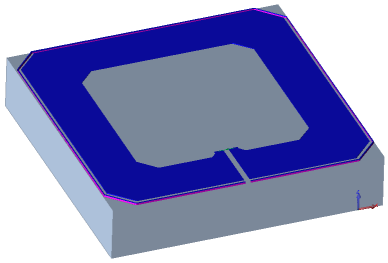

Fig. 2. Designed Inductor layout with its corresponding substrate.

A NOR-based ROM contains the fixed information, that is sent serially to the reader through load modulation. For this, a Parallel-Input Serial-Output (PISO) shift register is inserted between the memory outputs and the circuit output (Out) to transform the information from parallel to serial. The PISO shift register must capture the parallel memory bits, hold them and shift them on a clock by clock basis, all along the sequential logic through the output without losses. Consequently, a time limitation exists for converting the information from a parallel format to a serial format, that must be taken into account when designing this block. As it was mentioned, the PISO shift register is a synchronous block controlled by a clock signal from a 3-inverter ring oscillator. Besides this reference signal, load and shift signals must be implemented in order to convert the memory bits format. For this, a frequency divider signal, whose period is a multiple of the clock signal, is used to respect the load and shift times of the bit word. As both load and shift signals must be mutually exclusive, the same periodical signal can be used for both states to prevent bit losses. In other words, during half of the signal period memory bits are loaded into the PISO shift register, whereas, during the other half of the signal period, the bits are shifted in the direction of the output.

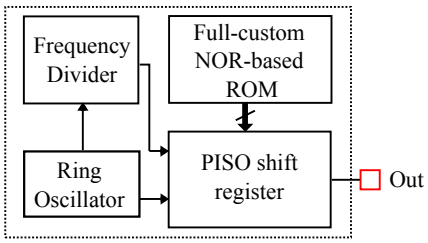

Fig. 3. ROM reading circuit diagram.

As it was mentioned, a low-power tag must be designed, therefore, the selected specifications to achieve this performance are defined in Table I.

III. Tag Integration

In order to attain a tag that can be incorporated to an RFID application, the memory reading circuit is connected to the designed inductor. In other words, the ROM reading circuit is considered as a load that must be powered through the inductor. However, to achieve this goal, a RF-DC front-end circuit must be added between the inductor and the load to rectify the received RF signal. The integrated tag diagram is presented in Fig. 4.

TABLE I
Tag Specification table.

Specification	Value
Load supply voltage	1 V
Load average power	4 μW
RF frequency signal	1.04 GHz
Backscattering frequency signal	1 MHz @ 1V

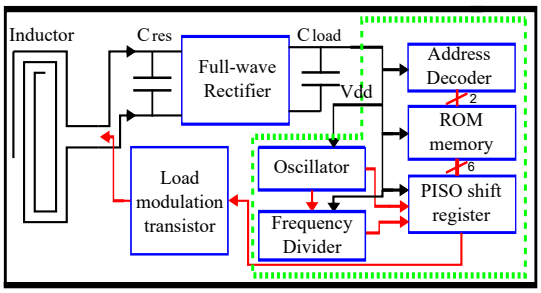

Fig. 4. Tag block diagram.

First of all, a resonating capacitor C_{res}, that acts as a matching network between the inductor and the full-wave rectifier, is connected in parallel with the inductor so as to achieve the resonance at the selected frequency. The full-wave rectifier converts the input RF signal into a DC voltage to energize the load.

In parallel with the load, there is a capacitance C_{load} that stores and then delivers energy to the load to satisfy the power peak demand when the circuit is switching. For test performance, an address decoder is added to the ROM reading circuit in order to select and access the different bit words stored in the memory. Finally, a load modulation transistor is utilized to communicate the data to the reader via backscattering.

IV. Results

To validate the performance of the tag, first, the electromagnetic simulation results of the simulated inductor are shown in order to extract its parasitic components and derive an electrical equivalent model. Then, the reading circuit results are presented to validate the concept and performance of the load. Finally, the simulation results of the integrated tag, including the parasitic structure model, are exhibited to validate the circuit.

A. Miniaturized inductor

An electromagnetic characterization of the full-custom inductor was realized in the Keysight® , Electromagnetic Professional (EMPro) EDA tool to obtain an extracted model. For this, the quality factor must be evaluated at the designed frequency with the respective real and imaginary parts of the

impedance as well. The corresponding frequency variation simulation results are presented in Fig. 5 and Fig. 6 respectively. As it was mentioned previously, a maximization of

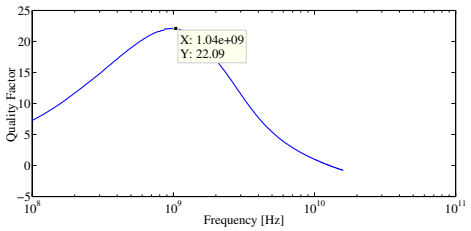

Fig. 5. Inductor quality factor as function of the frequency.

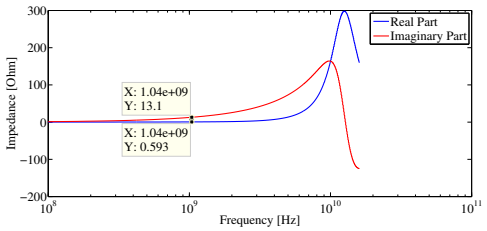

Fig. 6. Inductor real and imaginary impedance parts with frequency variation.

the quality factor is required for maximum power transfer efficiency. Based on this, Fig. 5 illustrates a maximum quality factor value of 22.09 at 1.04 GHz. From Fig. 6, it is possible to identify the real and imaginary impedance parts for the frequency of interest. The obtained values of the real and imaginary parts are approximately $\Re$(Z)=0.593 Ω and $\Im$(Z)= 13.1 Ω respectively. The imaginary part corresponds to an inductor value of 2 nH and the auto-resonance frequency is identified when the imaginary impedance value is null (transition from inductive behavior to capacitive behavior), which happens at a frequency of approximately 12 GHz. Therefore, the auto-resonance capacitor value is approximately 88 fF. The corresponding model of the inductor is presented in Fig. 7.

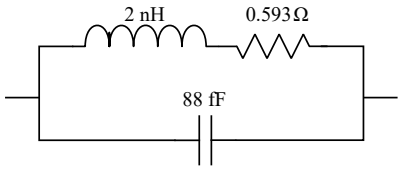

Fig. 7. Inductor parasitic extracted model.

Once the inductor model was extracted, a structural modeling of it can be included in Cadence Virtuoso to the integrated tag model for faster simulation results.

B. Memory Reading circuit

Four different word sequences were defined inside the ROM memory to have the possibility to select and transmit different information. The four sequences are defined in Table II with the respective input values combinations of the address decoder:

TABLE II
ADDRESS BIT WORDS TABLE.

A1 Value	A2 Value	Word Sequence
0 V	0 V	110101
0 V	1 V	110001
1 V	0 V	101111
1 V	1 V	101101

The corresponding results of the load system are presented in Fig. 8. In this figure are presented the inputs A0, A1 and the corresponding output (Vout) values. It is possible to identify the expected four different words associated to their respective inputs. In figure 8, from left to right are presented inside the dashed lines the sequences 101111, 110001, 110101 and 101101 respectively. As it can be identified, the load performance was validated with the obtained results. For power results validation, both static and dynamic power consumption for the different combinations are presented in Table III. The first one corresponds to the average power consumed by the load, whereas the second one is defined as the power demanded by the load when the circuit is switching.

TABLE III
STATIC AND DYNAMIC POWER FOR EACH INPUT COMBINATION.

Combination	Static Power [μW]	Dynamic Power [μW]
A0=0 V, A1=0 V	1.060	11.63
A0=1 V, A1=0 V	0.925	7.450
A0=0 V, A1=1 V	1.18	11.37
A0=1 V, A1=1 V	1.07	11.63

Consequently, the static power specification is accomplished based on the results presented above.

C. Integrated Tag

A parasitic extracted layout tag was simulated in order to append parasitic components to the performance of the circuit for a more accurate system behavior. The corresponding transient simulation results are presented in Fig. 9. In this figure, it is possible to identify the sequences 110101, 110001, 101111 and 101101 respectively. Based on this results, the bit sequences obtained corresponds to the expected ones.

Furthermore, a -4 dBm RF signal input power was determined after post-layout simulations for specification achievement.

The results from corners memory reading circuit simulation are presented in Table IV with the corresponding process, voltage and temperature variations (PVT). As it can be observed, the temperature range is greater than the supported by the human body, in order to also reach other applications besides biomedical implants. Based on the results, the static power specification was achieved.

Finally the miniaturized tag layout is presented in Fig. 10 occupying a 1.5 mm × 1.5 mm area.

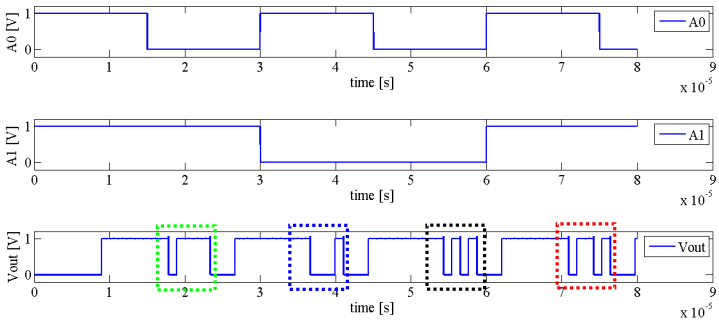

Fig. 8. Transient post-layout simulation of the load.

TABLE IV
CORNERS ANALYSIS.

Process	ff				ss				fs				sf			
Temperature [°C]	-40		80		-40		80		-40		80		-40		80	
Vdc [V]	0.8	1.2	0.8	1.2	0.8	1.2	0.8	1.2	0.8	1.2	0.8	1.2	0.8	1.2	0.8	1.2
Static Power [μW]	0.625	3.56	0.41	2.81	0.34	2.41	0.35	1.86	0.18	2.68	0.26	2.16	0.54	3.15	0.33	2.4
Dynamic Power [μW]	8.34	34.5	2.26	22.3	3.85	23.5	4.12	15.1	1.93	30.33	1.73	17.72	6.44	28.52	2.07	18.4

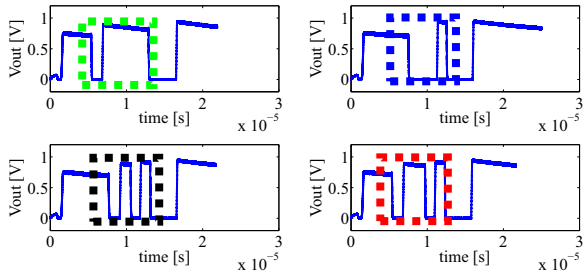

Fig. 9. Transient post-layout simulation of the tag.

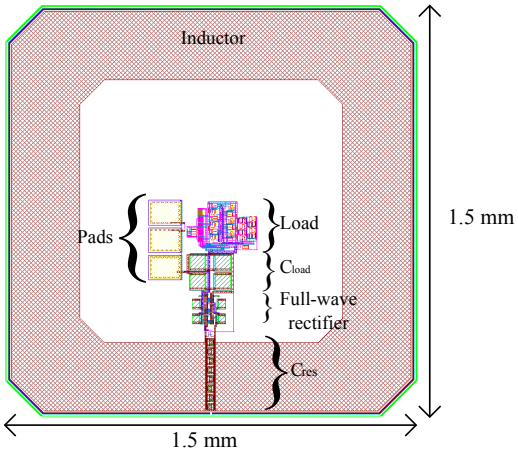

Fig. 10. Final layout of Tag.

V. CONCLUSION

A miniaturized on-chip antenna RFID tag that operates at 1.04 GHz, powered via inductive link with an embedded ROM reading circuit for biomedical applications was designed. This tag was fully developed in a 2.18 mm^2 area. The corresponding integration of the ROM-reading circuit and the inductor was attained and validated with simulations. An inductor layout model from EMPro was included in Cadence Virtuoso to achieve faster simulation results. Static power results were satisfied and dynamic power results were used to design correctly the corresponding load capacitor. The behavior of the circuit was also validated with simulation in corners for PVT variation.

ACKNOWLEDGMENT

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