DLL-based signal conditioning system for SAW sensor with digital output

R.E. Rottava, F. Rangel de Sousa✉ and S.M. Balashov

The use of a delay-locked loop (DLL) for conditioning signals from a surface acoustic wave (SAW) sensor is proposed. The system consists of a reference oscillator and a DLL. The signal generated in the reference oscillator is propagated through a sensitive SAW delay line (SAW-DL). The SAW propagating through this structure has a phase velocity dependent on environmental parameters such as temperature, humidity, mechanical deformation, or analyte concentration. Therefore, the system measures the physical quantity of interest by tracking the delay caused by the sensitive SAW-DL via a DLL. Fully digital DLL is made use of for the delay-tracking, which provides the conversion of the environmental parameter being sensed directly to the digital domain. The system is demonstrated through results from behavioural simulation, using a model of an SAW-DL sensitive to humidity.

Introduction: Electromechanical properties of surface acoustic wave delay lines (SAW-DLs) covered with sensitive thin films are known to be significantly sensitive to environmental parameters such as temperature, mechanical deformation, or analyte concentration. For instance, in [1] Caliendo *et al.* investigate the response of several chemical interactive material membranes to relative humidity (RH) on the exposure to water, ethanol, and acetone vapours. They report a considerable variation in the phase velocity and in the acoustic attenuation of signals propagating along the surface of the SAW-DL as function of the gas concentration. Recently, graphene oxide (GO) has been employed for enhancing the sensitivity of SAW-DL to humidity [2, 3].

The conventional conditioning circuit for SAW sensors consists of an RF oscillator including the SAW-DL with sensitive coat in the feedback loop [4]. The oscillation frequency is determined by the propagation velocity of the SAW-DL, which changes with the sensing parameter. This signal is then mixed with a signal from a reference oscillator (usually the same oscillator, but without the sensitive film), and the frequency difference is measured by a frequency counter. In a second approach [5], a voltage-controlled phase shifter (VCPS) is employed to phase-tune two feedback paths in order to establish a positive-feedback loop and allow oscillations to start. The voltage that controls the VCPS is then related to the RH.

In this Letter, we present a new conditioning system in which the sensitive SAW-DL operates in open-loop configuration. Therefore, the information about the environmental parameter under measure is conveyed in the delay of the signal propagating through the SAW structure, rather than in the frequency of an SAW oscillator. To track this delay, we employ a delay-locked loop (DLL) [6]. The DLL's control signal (filtered-error signal) follows the delay of the sensitive SAW-DL, and therefore allows a direct measure of the physical parameter being sensed. This proposed conditioning solution has the advantage of directly converting the physical quantity into a digital number, which can be easily post-processed in a digital signal processor without any intermediate conversion. Moreover, the fully digital structure has the advantages of low-area and low-power consumption.

Proposed system: The system we propose is presented in Fig. 1. A reference signal is generated by the reference oscillator, which is composed of a non-sensitive SAW-DL connected to an amplifier in positive-feedback configuration. The frequency of oscillation is independent (or nearly) from the environmental parameter we wish to sense. This reference signal is propagated through a sensitive SAW-DL and in parallel through a voltage-controlled DL (VCDL). The signals in the output of these blocks (*ssr* and *dln*, respectively) are phase-compared in the phase detector (PD), and the error signal is filtered in the loop filter. The filtered-error signal *ctr* is fed back to the VCDL where it controls the increment or decrement of the delay between *dln* and *osc*, in order to phase-align *dln* and *ssr*. Once the system reaches equilibrium, the time-delay difference between *dln* and *ssr* is kept constant, as long as perturbations are not too strong, and the blocks do not saturate. There is no restriction to the absolute amount of delay between *dln* and *ssr*, as long as it is kept constant throughout the operation. In fact, since the mechanical waves are much slower than the electric signals, *ssr* can reach a delay of hundreds of periods with respect to *dln*.

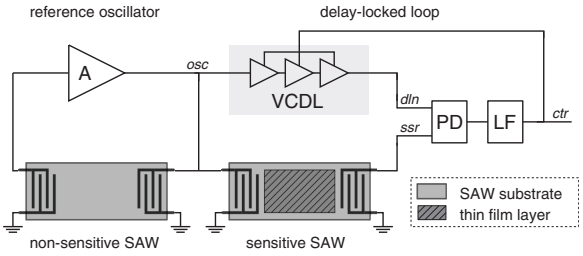

Fig. 1 *Proposed conditioning system for SAW sensors*

The main perturbation of this feedback system arises from environmental parameters (humidity, temperature, gas concentration etc.) which modify the delay caused by the sensitive SAW-DL. The interaction between the environment and the thin-layer deposited onto the surface of the SAW-DL can be described by a continuous and smooth function, which causes a slow variation in the delay of the sensitive SAW-DL, in the order of seconds [1]. The two separated SAW-DL structures of Fig. 1 can be fabricated over a single substrate, providing a better thermal stability and lower power consumption [5].

In the next section, we discuss a fully digital implementation of the DLL. The design of reference SAW oscillators is fully covered in other references [1, 2].

Fully digital DLL: Fig. 2 presents the fully digital DLL. It is composed of saturation amplifiers, a D flip-flop, a divide-by-K frequency divider, an M-bit counter, and a digital-controlled DL (DCDL) built from delay blocks Δ_0 to Δ_{M-1}. The signals arriving from the reference oscillator (*osc*) and from the sensitive SAW-DL (*ssr*) are digitised through a saturation operation. Therefore, the signals in the DLL are all digital, as well as the control logic, which qualifies this circuit as fully digital. Each delay block of the DCDL is composed of a number of delay elements, which increases by a power of two at each level. A delay element can be realised by a digital inverter and a few switches to choose between a delay path (δ seconds of delay) and a non-delay path (0 s of delay). This implementation circumvents the use of varactors for controlling the DCDL delay, avoiding undesired non-linear effects. This is important because the conversion gain is directly related to the transfer function of the DL.

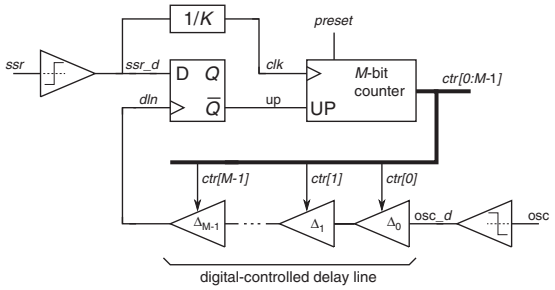

Fig. 2 *Fully digital implementation of DLL for conditioning circuit*

The total time-delay is given by

$$\tau = \tau_{\Delta_0} + \tau_{\Delta_1} + \cdots + \tau_{\Delta_n}, \tag{1}$$

where the time-delay of the nth delay block is

$$\tau_{\Delta_n} = \begin{cases} 0 & ctr[n] = '0', \\ 2^n\delta & ctr[n] = '1'. \end{cases} \tag{2}$$

The parameter δ characterises one delay element. The DL is controlled by the M-bit digital word *ctr*, which ranges from 0 up to $2^M - 1$. This input digital word is mapped to a delay in the range $[0,\ (2^M - 1)\delta]$, with step size δ. Therefore, the DL covers $(2^M - 1)\delta/T_{\text{osc}}$ periods, with steps of δ/T_{osc} periods, where T_{osc} is the fundamental period of the reference signal osc. The response of the transducer (maximum delay variation) and the accuracy required in the measurement will determine the maximum value of δ and minimum number of blocks in the DCDL.

The phase detection is performed by the D flip-flop: if the signal *ssr_d* is high at the rising of *dln*, it means the first signal is phase-advanced in relation to the second, which generates the flag $up = '0'$; otherwise, it

means *dln* is phase-advanced in relation to *ssr_d*, which generates the flag $up = '1'$. This phase detection is binary, i.e. *dln* is either phase-advanced or phase-delayed. The range of this detector is $\pm\pi$, and it requires that the signal *ssr_d* presents 50% duty-cycle. Finally, the precision of the phase detection is a function of the guard times of the D flip-flop (setup time and hold time).

The *M*-bit counter serves as an accumulator. At each rising edge of *clk,* the digital word *ctr* is incremented by 1 if $up = '1'$ and decremented by 1 if $up = '0'$. The accumulator is set to an initial condition through the signal *preset*, which is internally configured to set *ctr* to the mid-point ($2^M/2$) in order to allow the system to swing in both directions, increasing or decreasing the delay of the DL. The accumulator is updated in a rate *K* times lower than the rate of the *ssr_d* signal. This lower rate is determined by the transient response of the sensitive SAW-DL.

When the operation of the DLL starts, the accumulator is set to a predetermined initial condition via *preset*. At each rising edge of *clk*, the system updates to a state where the phase difference between *ssr_d* and *dln* is smaller, until it reaches equilibrium. In the steady-state condition there will always be an least significant bit (LSB) error in the digital word *ctr* due to the binary operation of the PD. For instance, if the *dln* rising edge happens before the *ssr_d* rising edge, the next state of the accumulator is incremented by 1, which increases the time-delay of the DL by one step (δ). Then, in the next cycle the edge of *dln* will happen after *ssr_d*, decreasing by 1 the next state of the accumulator, and consequently decreasing the time-delay of the DL by one step. This quantisation error is present in any digital acquisition system.

The system remains locked as long as variations in the delay of *ssr_d* are slow enough to track, and as long as the accumulator is within its operation range $[0,\ 2^M - 1]$. A common issue in feedback systems is the saturation of the integrator, or in this case the accumulator, which drives the system to an unlock condition. This situation has to be avoided by proper designing.

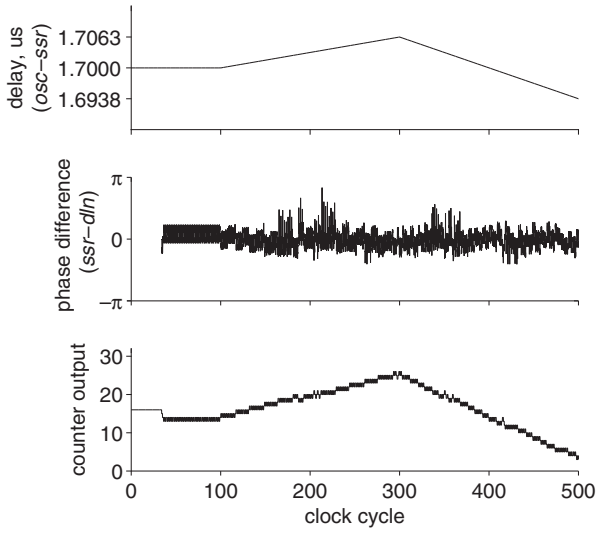

Fig. 3 *Behavioural simulation results of fully digital DLL (RH sensor)*

System implementation: The functionality of this system is demonstrated by behavioural simulation in Verilog-A, using the model of an SAW-DL sensitive to RH. The simulated sensitive SAW-DL has a centre frequency of 160 MHz, and a dynamic range of two fundamental periods T_{osc}, i.e. the delay difference between 0% RH and 100% is equivalent to two periods of the reference signal. Therefore, the VCDL is required to cover at least $2T_{osc}$ of delay. We chose to cover $3T_{osc}$ of delay, with an accumulator resolution *M* of 5 bits, which then requires a delay step δ of $3T_{osc}/(2^M - 1) \approx 605$ ps. The reference frequency is divided by $K = 8$ to generate the *clk* signal, which allows enough time for the system to stabilise in a new state, and is still fast enough to track any perturbation in the delay of the sensitive SAW-DL. As a matter of fact, *K* could have been set much higher (e.g. 1024) and the DLL would still track perturbations, since transitions in the delay of the SAW-DL are in the order of seconds.

The simulation results of the DLL behavioural model are presented in Fig. 3. The first plot depicts the time-delay added by the sensitive SAW-DL. It starts with a constant delay of 1.7 µs (which was obtained experimentally from an SAW-DL coated with GO). From the 100–500th clock cycle, the delay increases to 1.7 µs + T_{osc} and then decreases to 1.7 µs − T_{osc}. At the beginning of the operation, the accumulator is initialised to 16. Once the DLL is locked, the mean of the phase difference between *ssr* and *dln* is kept close to zero, and peak values never exceed $\pm\pi$. The output value of the accumulator represents the amount of excess delay added by the sensitive SAW-DL, which is caused by variations in the RH of the environment. The system can track variations of $\pm T_{osc}$ in the delay of the sensitive SAW-DL.

Conclusion: In this Letter, we proposed a novel conditioning system for SAW sensors. A fully digital DLL is employed to track the delay added to a reference signal by a sensitive SAW-DL, which is sensible to environmental parameters. The system demonstrates capability of sensing temperature, humidity, and concentration of some specific gases. One of the main advantages of this conditioner is a direct conversion from the physical quantity to the digital domain. A humidity sensor was modelled in Verilog-A and simulated as a case study. The simulation results demonstrate the expected performance of the system.

Acknowledgments: This study has been supported by the National Council for Scientific and Technological Development (CNPq) and by the Instituto Nacional de Ciência e Tecnologia de Sistemas Micro e Nanoeletrônicos (Science and Technology National Institute of Micro and Nanoelectronic Systems) (INCT NAMITEC).

Submitted: *16 February 2016*
doi: 10.1049/el.2016.0529

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